HIGH - PERFORMANCE
BiCMOS
DATA BOOK

Saratoga Semiconductor

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BiCMOS
DATA
BOOK

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Printed in U.S.A. 9/88

Saratoga's broad line of products provide very high performance BiCMOS solutions to designers of high performance digital systems. Our products include industry standard devices as well as products with performance, drive, density, package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

Use this book to find ordering information. Start with the Table of Contents to locate the product of interest. Then refer to the Ordering Information Chart at the back of each datasheet to locate the exact Saratoga part number in question.

Use this book to find product data. Start with the Table of Contents, organized either alphanumerically by product line or numerically across all products. For a more complete summary of product line offerings, use the Product Selector Guide. These indexes will direct you to the page on which the complete technical data sheet can be found. Data Sheets may be of the following type:

PRELIMINARY INFORMATION: contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

ADVANCE INFORMATION: contain descriptions for products soon to be or recently released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL: contain minimum and maximum limits specified over the complete supply and temperature range of full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local Saratoga sales representative or call 408-522-7500 to determine latest device specifications, package types and product availability.

Published September 30, 1988

Saratoga Semiconductor

TABLE OF CONTENTS

PRODUCTS AND CAPABILITIES

QUALITY AND RELIABILITY

BiCMOS TTL SRAMS

BiCMOS TTL CACHE TAGS

BiCMOS TTL FIFO'S

BiCMOS TTL LOGIC

BiCMOS TTL MODULES

BiCMOS ECL SRAMS

PACKAGING

PACKAGING

SALES OFFICES

PRODUCTS AND CAPABILITIES

SARATOGA BACKGROUND

Saratoga Semiconductor, founded in September of 1985, designs, manufactures and markets ultra-high performance integrated circuits for applications in computer, work-station, telecommunications, data communications, instrumentation and military markets. The company is the first in the United States to mass produce high-end, large scale BiCMOS integrated circuits utilizing a proprietary process technology called SABiC (Self-Aligned Bipolar CMOS). Emerging rapidly with wide acceptance, BiCMOS is considered the most viable vehicle to compliment CMOS and Bipolar technologies to provide integrated circuits with fast switching speed, high current drive, high density and low power consumption.

Privately held, Saratoga Semiconductor has raised a total $28.5 million in three rounds of funding. The original Cupertino, California facilities consists of some 30,000 sq-ft which includes a 10,000 sq-ft class 10 Fab. In order to sustain the planned business growth, at press time, the company is in the process of moving its entire facilities from the existing Cupertino office and Fab to a 67,000 sq-ft twin-building in Sunnyvale, California. The new Fab (also class 10), will be equipped with two wafer processing lines by the end of 1988, boosting total wafer processing capacity to more than three times the current run rate. The total move is expected to be completed before the end of 1988.

Saratoga Semiconductor participates exclusively in the high performance segment of the semiconductor market. With BiCMOS, the company is fully dedicated to providing both TTL and ECL I/O compatible products to satisfy a broad spectrum of applications requirements, particularly those in 32-bit CISC and RISC based systems and high performance super-minicomputers. As for new products, the company is committed to a strategy to:

(1) Close the speed gap between CPU and main memory by providing the fastest data cache, instruction cache and cache tag memories.

(2) Unplug the I/O bottleneck with the fastest FIFO memories and bus interface products.

(3) Ease system design with new generations of intelligent SRAMS.

(4) Enhance the driving of heavily loaded system buses with high current drive BiCMOS products.

(5) Improve and protect data integrity by providing error detection and correction circuits.

(6) Sustantially increase performance/density by offering a wide range of very dense SRAM and FIFO modules.

In the long term, the company will dedicate significant resources to addressing the burgeoning market for RISC support chip-sets.

Consistent with the above strategy, Saratoga's product offerings in 1988 consists of four major families. They are TTL static RAMs, ECL static RAMs, TTL First-In-First-Out Memories and cache tag memories. These products are to be supplemented by Dual-port ECL SRAMs, synchronous (self-timed) TTL SRAMs, TTL SRAM Modules and logic LSI products in late 1988 and early 1989.

In the past decade, significant progress had been made in the IC industry. During that period, gate speed went from 10ns to 1ns, circuit density jumped from 50,000 to 350,000 transistors, power dissipation per gate has been reduced by a factor of five, and surface mount packaging gained wide acceptance. Furthermore, and most important of all, the cost per bit for memory continues to decline.

In the ultra-high performance arena, Bipoloar ECL, though delivering the needed speed, is deemed to be too power hungry for economical and reliable operation as a mainstream technology. On the other hand, CMOS technology while contributing greatly in providing higher integration and low power consumption, has reached the point of diminishing return in terms of squeezing further speed improvement and off chip drive. These trade-off issues are very difficult to resolve until the advent of a process technology which could combine the attributes of Bipolar and CMOS. These attributes can be summarized as those that offer the system designers ultra fast switching speed, low power consumption, high current drive and a high level of integration. BiCMOS is an emerging technology which fulfills the mainstream demand of the system designes. BiCMOS, if properly applied, can produce products that are compatible with the high performance demands of all the latest in 32-bit CISC and RISC processors.

Saratoga Semiconductor developed a proprietary BiCMOS process technology, known as SABiC (Self-Aligned Bipolar CMOS). Within the last year, Saratoga has quickly gained the leadership position as the first manufacturer in the United States to mass produce ICs solely based on this process.

A typical BiCMOS device cross section is shown in Figure 1. Basic device structural features include the following:

- **Semi-recessed Oxide Isolation**
- **P-Epi on P-substrate**
- **Bipolar Device:**
  Base width <0.15um
  Extended electrode, poly contact
- **CMOS Device**
  Channel length drawn: 1.5um
- **Double Poly, Double Metal**

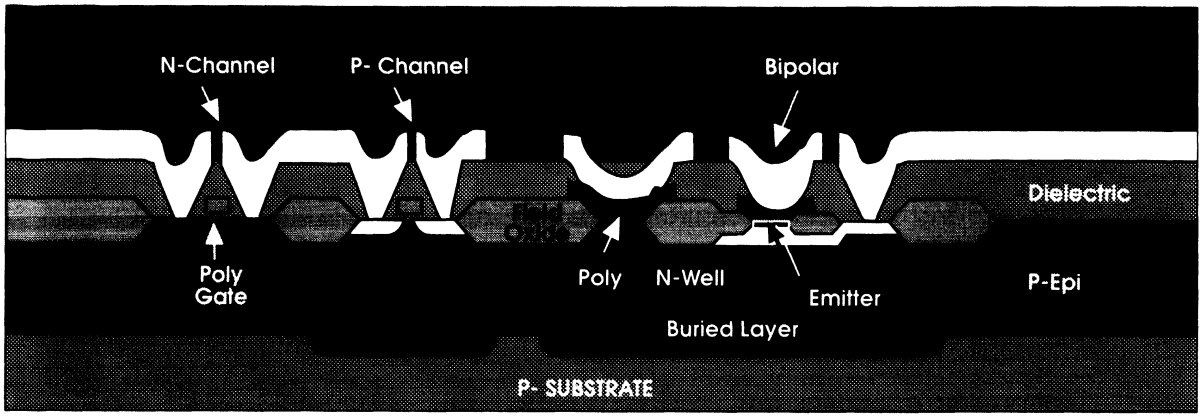

Figure 1. Typical BiCMOS Device Cross Section

Working with conservative geometry as mentioned above, BiCMOS technology is capable of producing ICs with speed comparable to or greater than that of CMOS processes of more aggressive design rules in the 1.0 um or 0.8 um range. In addition, BiCMos tends to have a very tight yield-distribution curve. Therefore, it is expected that BiCMOS can be as cost effective as CMOS for applications within the ultra-high speed range of 25ns or less. In the next two years, gradual scaling of BiCMOS will further shrink the CMOS portion and speed up the cut-off frequency of the bipolar device to 10 or 11 GHz.

BiCMOS is a versatile technology where the mixing of analog and digital circuitry on the same chip is possible. This capability will open up new applications in data acquisition, color graphics, imaging and fiber optics communications for the next few years.

Due to the high performance nature of Saratoga's BiCMOS products, each product line targets a different functional application within a computer environment.

The TTL and ECL static RAM family finds wide acceptance as data and instruction cache in the CPU; look-up table for high resolution graphics systems and writeable control store for micro-programmable systems.

The FIFO family is invaluable for applications such as real time data acquisition, telemetry, telecommunications, inter-processor data buffering, local area network mail-box buffer, peripheral to peripheral data buffer. Saratoga was the first to intoduce 50 MHz FIFOs. This remains unchallenged.

Cache tag memories are used universally in high bandwidth, 32-bit CISC and RISC systems, performing the vital function of tag comparison. Being in the most speed critical loop of the processor, the cache tag's fast address compare function can directly impact system performance. Saratoga is the first to produce a 15ns cache tag and has claimed many design-ins with the Motorola 68030, Intel 80386 and the SPARC., to mention a few.

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COMMERCIAL SELECTION GUIDE

FAMILY	DENSITY	DEVICE FEATURES/ORGANIZATION	CT	DEVICE NO.	DEVICE SPEED (ns)	I_{CC} (mA)	STATUS	PACKAGES	COMMENTS
BiCMOS TTL SRAMs	4K	1K x 4 - CS Power Down	18	SSM2148	t_{AA} = 15,20,25	50	F	P, C	
	4K	1K x 4	18	SSM2149	t_{AA} = 15,20,25	50	F	P, C	
	4K	1K x 4 - Separate I/O	24	SSM2150	t_{AA} = 15,20,25	TBD	P	P, S	
	16K	16K x 1	20	SSM6167	t_{AA} = 20,25,35	60	F	C	
	16K	4K x 4	20	SSM6168	t_{AA} = 20,25,35	90	F	P, E, S	
	16K	4K x 4 - Output Enable	22	SSM6170	t_{AA} = 20,25,35	90	F	P, D, E, S	
	16K	4K x 4 - Separate I/O, Transparent Write	24	SSM6171	t_{AA} = 20,25,35	90	F	P, D, E, S	
	16K	4K x 4 - Separate I/O	24	SSM6172	t_{AA} = 20,25,35	90	F	P, D, E, S	
	16K	2K x 8	24	SSM6116	t_{AA} = 20,25,35	120	F	P, D, E, S	
	64K	16K x 4 - Separate I/O, Transparent Write	28	SSM7161	t_{AA} = 20,25,35	125	F	P, S	
	64K	16K x 4 - Separate I/O	28	SSM7162	t_{AA} = 20,25,35	125	F	P, S	
	64K	16K x 4 - Output Enable	24	SSM7166	t_{AA} = 20,25,35	125	F	P, S	
	64K	16K x 4	22	SSM7188	t_{AA} = 20,25,35	125	F	P, S	
	64K	16K x 4 - Output Enable, Dual CS	24	SSM7198	t_{AA} = 20,25,35	125	F	P, S	
	64K	8K x 8	28	SSM7164	t_{AA} = 20,25,35	150	F	P, S	
	64K	16K x 4 - SIO, Latched Outputs	28	SSM7192	t_{AA} = 20,25,30,35	TBD	P	S	
	64K	16K x 4 - SIO, Registered Outputs	28	SSM7193	t_{AA} = 20,25,30,35	TBD	P	S	
	64K	16K x 4 - SIO, Latched Outputs, OE	28	SSM7194	t_{AA} = 20,25,30,35	TBD	P	S	
	64K	16K x 4 - SIO, Registered Outputs, OE	28	SSM7195	t_{AA} = 20,25,30,35	TBD	P	S	
BiCMOS TTL CACHE TAGS	16K	4K x 4 -Cache Tag, Totem-Pole Outputs	22	SSL4180	t_{Ω} (A) = 15,20,25,35	110	A	P, S	
	16K	4K x 4 -Cache Tag, Open Drain Outputs	22	SSL4181	t_{Ω} (A) = 15,20,25,35	110	A	P, S	
	18K	2K x 9 -Cache Tag, Totem-Pole Outputs	28	SSL2152	t_{DCA} = 20,25,30	125	A	P, C	
	18K	2K x 9 -Cache Tag, Open Drain Outputs	28	SSL2154	t_{DCA} = 20,25,30	125	A	P, C	
BiCMOS TTL FIFOs	256	64 x 4 - Cascadeable	16	SSL7401	f_0 = 50,40,25,15,10 MHz	75	A	P, C	
	256	64 x 4 - Cascadeable, OE	16	SSL7403	f_0 = 50,40,25,15,10 MHz	75	A	P, C	
	320	64 x 5 - Cascadeable	18	SSL7402	f_0 = 50,40,25,15,10 MHz	75	A	P, C	
	320	64 x 5 - Cascadeable, OE	18	SSL7404	f_0 = 50,40,25,15,10 MHz	75	A	P, C	
	320	64 x 5 - Cascadeable, Flags	20	SSL7413	f_0 = 50,40,35,25,15 MHz	90	A	P, C	
	512	64 x 8 - Cascadeable, OE	28	SSL7408	f_0 = 50,40,35,25,15MHz	135	A	P, S	
	576	64 x 9 - Cascadeable	28	SSL7409	f_0 = 50,40,35,25,15MHz	135	A	P, S	
	2304	256 x 9 - Cascadeable, Flags	28	SSL7200A	t_A = 15,25,35,50=	100	A	P, C	300/600 MIL PDIP
	2304	256 x 9 - Cascadeable, Flags, OE	28	SSL7200B	t_A = 15,25,35,50	100	A	P, C	300/600 MIL PDIP
	2304	128 x 18 - 18 Bit/18 Bit Ports, Flags	68	SSL72434	t_{DA} = 10	TBD	P	J, A	
	4096	128 x 32 - 32 Bit/32 Bit Ports, Flags	84	SSL72432	t_{DA} = 10	TBD	P	J, A	
	4608	128 x 36 - 18 Bit/36 Bit Ports, Flags	84	SSL72435	t_{DA} = 10	TBD	P	J, A	
	4608	128 x 36 - 36 Bit/36 Bit Ports, Flags	120	SSL72436	t_{DA} = 10	TBD	P	A	
	4608	512 x 9 - Cascadeable	28	SSL7201	t_A = 15,25,35,50	100	A	P, C	300/600 MIL PDIP
	4608	512 x 9 - Cascadeable, Flags	28	SSL7201A	t_A = 15,25,35,50	100	A	P, C	300/600 MIL PDIP
	4608	512 x 9 - Cascadeable, Flags, OE	28	SSL7201B	t_A = 15,25,35,50	100	A	P, C	300/600 MIL PDIP
	9216	1K x 9 - Cascadeable	28	SSL7202	t_A = 15,25,35,50	100	A	P, C	300/600 MIL PDIP
	9216	1K x 9 - Cascadeable, Flags	28	SSL7202A	t_A = 15,25,35,50	100	A	P, C	300/600 MIL PDIP
	9216	1K x 9 - Cascadeable, Flags, OE	28	SSL7202B	t_A = 15,25,35,50	100	A	P, C	300/600 MIL PDIP
	18432	2K x 9 - Cascadeable	28	SSL7203	t_A = 15,25,35,50	100	A	P, C	600 MIL PDIP
	18432	2K x 9 - Cascadeable, Flags	28	SSL7203A	t_A = 15,25,35,50	100	A	P, C	600 MIL PDIP
TTL LOGIC	NA	32-Bit Error Detection & Correction Unit	68	SSL29660	t_D /t_C = 16/24	TBD	P	J, L, A	
BiCMOS TTL MODULES	256K	32K x 8 -SRAM	28	SSB91256	t_{AA} = 25,30,35	TBD	P	G	600 MIL PDIP Compatible
	256K	16K x 16 -SRAM, OE	40	SSB91257	t_{AA} = 20,25,30	TBD	P	H, Z	SIP/ZIP
	256K	16K x 16 -SRAM	40	SSB91258	t_{AA} = 20,25,30	TBD	P	H, Z	SIP/ZIP
	256K	16K x 16 -SRAM, OE, Dual CS	40	SSB91259	t_{AA} = 20,25,30	TBD	P	H, Z	SIP/ZIP
	256K	16K x 16 -SRAM	40	SSB91260	t_{AA} = 20,25,30	TBD	P	H	SIP
	512K	16K x 32 -SRAM, OE	60	SSB91512	t_{AA} = 20,25,30	TBD	P	Z	ZIP
	512K	16K x 32 -SRAM	60	SSB91513	t_{AA} = 20,25,30	TBD	P	Z	ZIP
	512K	16K x 32 -SRAM, OE, Dual CS	60	SSB91514	t_{AA} = 20,25,30	TBD	P	Z	ZIP
BiCMOS ECL SRAMs	4K	4K x 1 - 10K/10KH Compatible	18	SSM10470	t_{AA} = 10,15	195	F	C	
	4K	4K x 1 - 100K Compatible	18	SSM100470	t_{AA} = 10,15	195	F	C	
	4K	1K x 4 - 10K/10KH Compatible	24	SSM10474	t_{AA} = 8,10,15	240	F	C	
	4K	1K x 4 - 100K Compatible	24	SSM100470	t_{AA} = 8,10,15	240	F	C	
	16K	16K x 1 - 10K/10KH Compatible	20	SSM10480	t_{AA} = 10,15	195	F	C	
	16K	16K x 1 - 100K Compatible	20	SSM100480	t_{AA} = 10,15	195	F	C	
	16K	4K x 4 - 10K/10KH Compatible	28	SSM10484	t_{AA} = 10,15	220	F	S	
	16K	4K x 4 - 100K Compatible	28	SSM100484	t_{AA} = 10,15	220	F	S	
	64K	16K x 4 - 10K/10KH Compatible	28	SSM10494	t_{AA} = 15,20	TBD	P	S	
	64K	16K x 4 - 100K Compatible	28	SSM100494	t_{AA} = 15,20	TBD	P	S	

NOTES: The specifications above are for the Commercial Temperature Range of 0°C to 70°C.
Military Temperature Range (-55 °C to +125 °C) and MIL-STD 883C Level B product are listed on the next page.
F, J, L and X configurations are available through special order only, please contact factory.

Family Designator	Package Designator				Data Sheet Status
L: Logic	**A:** Pin grid Array	**E:** Plastic SOJ (J-Lead)	**J:** PLCC	**X:** Die	**P:** Preliminary
M: Memory	**C:** Ceramic DIP	**F:** Flat Package	**L:** Ceramic LCC	**Z:** Plastic ZIP Module	**A:** Advance Information
B: Module	**D:** Plastic SOIC (Gull-Wing)	**G:** Plastic DIP Module	**P:** Plastic DIP		**F:** Final
		H: Plastic SIP Module	**S:** Sidebraze DIP		

Saratoga Semiconductor

MILITARY SELECTION GUIDE

FAMILY	DENSITY	DEVICE FEATURES/ORGANIZATION	CT	DEVICE NO.	DEVICE SPEED (ns)	I_{CC} (mA)	STATUS	PACKAGES	COMMENTS
BiCMOS TTL SRAMs	4K	1K x 4 - CS Power Down	18	SSM2148	t_{AA} = 20,25,35	50	F	C	
	4K	1K x 4	18	SSM2149	t_{AA} = 20,25,35	50	F	C	
	4K	1K x 4 - Separate I/O	24	SSM2150	t_{AA} = 20,25,35	TBD	P	S	883C
	16K	16K x 1	20	SSM6167	t_{AA} = 25,35,45	60	F	C	
	16K	4K x 4	20	SSM6168	t_{AA} = 25,35,45	90	F	S	
	16K	4K x 4 - Output Enable	22	SSM6170	t_{AA} = 25,35,45	90	F	S	
	16K	4K x 4 - Separate I/O, Transparent Write	24	SSM6171	t_{AA} = 25,35,45	90	F	S	883C
	16K	4K x 4 - Separate I/O	24	SSM6172	t_{AA} = 25,35,45	90	F	S	883C
	16K	2K x 8	24	SSM6116	t_{AA} = 25,35,45	120	F	S	883C
	64K	16K x 4 - Separate I/O, Transparent Write	28	SSM7161	t_{AA} = 25,35,45	125	F	S	883C
	64K	16K x 4 - Separate I/O	28	SSM7162	t_{AA} = 25,35,45	125	F	S	883C
	64K	16K x 4 - Output Enable	24	SSM7166	t_{AA} = 25,35,45	125	F	S	883C
	64K	16K x 4	22	SSM7188	t_{AA} = 25,35,45	125	F	S	883C
	64K	16K x 4 - Output Enable, Dual CS	24	SSM7198	t_{AA} = 25,35,45	125	F	S	883C
	64K	8K x 8	28	SSM7164	t_{AA} = 25,35,45	150	F	S	883C
	64K	16K x 4 - SIO, Latched Outputs	28	SSM7192	t_{AA} = 20,25,30,45	TBD	P	S	
	64K	16K x 4 - SIO, Registered Outputs	28	SSM7193	t_{AA} = 20,25,30,45	TBD	P	S	
	64K	16K x 4 - SIO, Latched Outputs, OE	28	SSM7194	t_{AA} = 20,25,30,45	TBD	P	S	
	64K	16K x 4 - SIO, Registered Outputs, OE	28	SSM7195	t_{AA} = 20,25,30,45	TBD	P	S	
BiCMOS TTL CACHE TAGS	16K	4K x 4 -Cache Tag, Totem-Pole Outputs	22	SSL4180	t_{α} (A) = 20,25,35,45	TBD	P	S	
	16K	4K x 4 -Cache Tag, Open Drain Outputs	22	SSL4181	t_{α} (A) = 20,25,35,45	TBD	P	S	
	18K	2K x 9 -Cache Tag, Totem-Pole Outputs	28	SSL2152	t_{DCA} = 20,25,35,45	TBD	P	C	
	18K	2K x 9 -Cache Tag, Open Drain Outputs	28	SSL2154	t_{DCA} = 20,25,35,45	TBD	P	C	
BiCMOS TTL FIFOs	256	64 x 4 - Cascadeable	16	SSL7401	f_0 = 50,40,25,15,10 MHz	90	A	C	
	256	64 x 4 - Cascadeable, OE	16	SSL7403	f_0 = 50,40,25,15,10 MHz	90	A	C	
	320	64 x 5 - Cascadeable	18	SSL7402	f_0 = 50,40,25,15,10 MHz	90	A	C	
	320	64 x 5 - Cascadeable, OE	18	SSL7404	f_0 = 50,40,25,15,10 MHz	90	A	C	
	320	64 x 5 - Cascadeable, Flags	20	SSL7413	f_0 = 50,40,35,25,15 MHz	100	A	S	883C
	512	64 x 8 - Cascadeable, OE	28	SSL7408	f_0 = 50,40,35,25,15MHz	140	A	S	883C
	576	64 x 9 - Cascadeable	28	SSL7409	f_0 = 50,40,35,25,15MHz	140	A	C	
	2304	256 x 9 - Cascadeable, Flags	28	SSL7200A	f_A = 25,35,50,65	120	A	C	
	2304	256 x 9 - Cascadeable, Flags, OE	28	SSL7200B	f_A = 25,35,50,65	120	P	A	
	2304	128 x 18 - 18 Bit/18 Bit Ports, Flags	68	SSL72434	TBD	TBD	P	A	
	4096	128 x 32 - 32 Bit/32 Bit Ports, Flags	84	SSL72432	TBD	TBD	P	A	
	4608	128 x 36 - 18 Bit/36 Bit Ports, Flags	84	SSL72435	TBD	TBD	P	A	
	4608	128 x 36 - 36 Bit/36 Bit Ports, Flags	120	SSL72436	TBD	TBD	P	A	
	4608	512 x 9 - Cascadeable	28	SSL7201	f_A = 25,35,50,65 MHz	120	A	C	
	4608	512 x 9 - Cascadeable, Flags	28	SSL7201A	f_A = 25,35,50,65 MHz	120	A	C	
	4608	512 x 9 - Cascadeable, Flags, OE	28	SSL7201B	f_A = 25,35,50,65 MHz	120	A	C	
	9216	1K x 9 - Cascadeable	28	SSL7202	f_A = 25,35,50,65 MHz	120	A	C	
	9216	1K x 9 - Cascadeable, Flags	28	SSL7202A	f_A = 25,35,50,65 MHz	120	A	C	
	9216	1K x 9 - Cascadeable, Flags, OE	28	SSL7202B	f_A = 25,35,50,65 MHz	120	A	C	
	18432	2K x 9 - Cascadeable	28	SSL7203	f_A = 25,35,50,65 MHz	120	A	C	
	18432	2K x 9 - Cascadeable, Flags	28	SSL7203A	f_A = 25,35,50,65 MHz	120	A	C	
TTL LOGIC	NA	32-Bit Error Detection & Correction Unit	68	SSL29660	TBD	TBD	P	L,A	
BiCMOS TTL MODULES	256K	32K x 8 -SRAM	28	SSB91256	t_{AA} = 30,35,45	TBD	P	TBD	
	256K	16K x 16 -SRAM, OE	40	SSB91257	t_{AA} = 25,30,35	TBD	P	TBD	
	256K	16K x 16 -SRAM	40	SSB91258	t_{AA} = 25,30,35	TBD	P	TBD	
	256K	16K x 16 -SRAM, OE, Dual CS	40	SSB91259	t_{AA} = 25,30,35	TBD	P	TBD	
	256K	16K x 16 -SRAM	40	SSB91260	t_{AA} = 25,30,35	TBD	P	TBD	
	512K	16K x 32 -SRAM, OE	60	SSB91512	t_{AA} = 25,30,35	TBD	P	TBD	
	512K	16K x 32 -SRAM	60	SSB91513	t_{AA} = 25,30,35	TBD	P	TBD	
	512K	16K x 32 -SRAM, OE, Dual CS	60	SSB91514	t_{AA} = 25,30,35	TBD	P	TBD	
BiCMOS ECL SRAMs	4K	4K x 1 - 10K/10KH Compatible	18	SSM10470	TBD	TBD	P	C	
	4K	4K x 1 - 100K Compatible	18	SSM100470	TBD	TBD	P	C	
	4K	1K x 4 - 10K/10KH Compatible	24	SSM10474	TBD	TBD	P	C	
	4K	1K x 4 - 100K Compatible	24	SSM100470	TBD	TBD	P	C	
	16K	16K x 1 - 10K/10KH Compatible	20	SSM10480	TBD	TBD	P	C	
	16K	16K x 1 - 100K Compatible	20	SSM100480	TBD	TBD	P	C	
	16K	4K x 4 - 10K/10KH Compatible	28	SSM10484	TBD	TBD	P	S	
	16K	4K x 4 - 100K Compatible	28	SSM100484	TBD	TBD	P	S	
	64K	16K x 4 - 10K/10KH Compatible	28	SSM10494	TBD	TBD	P	S	
	64K	16K x 4 - 100K Compatible	28	SSM100494	TBD	TBD	P	S	

NOTES: The specifications above are for the Military† Temperature Range of -55°C to +125°C.
Military Temperature Range (-55 °C to +125 °C) and MIL-STD 883C Level B product are both listed on this next page.Level B devices can be identified by the 883C listed in the comments section. All other are MIL Temp devices but are capable of being tested via Group A, B, C, D to 883C compliance.
F, L and X configurations are available through special order only, please contact factory.

Family Designator	Package Designator				Data Sheet Status
L: Logic	**A:** Pin grid Array	**E:** Plastic SOJ (J-Lead)	**J:** PLCC	**X:** Die	**P:** Preliminary
M: Memory	**C:** Ceramic DIP	**F:** Flat Package	**L:** Ceramic LCC	**Z:** Plastic ZIP Module	**A:** Advance Information
B: Module	**D:** Plastic SOIC (Gull-Wing)	**G:** Plastic DIP Module	**P:** Plastic DIP		**F:** Final
		H: Plastic SIP Module	**S:** Sidebraze DIP		

ORDERING INFORMATION

Specific ordering codes are indicated in the detailed data sheets.
In general, the product codes follow the format below:

CAGE Code/FSCM Number: OCTG5
Minimum Order Amount: $100.00

S S M 6116 - 25 P C

Operating Range and Screening Procedures Designator

- **C**: 0 to +70 °C Commercial Processing
- **B**: -55 to +125 °C MIL-STD-883C, Class B
- **M**: -55 to +125 °C
- **S**: 25 °C Only Engineering Samples

Package Designator

- **A**: Pin Grid Array
- **C**: Ceramic DIP
- **D**: Plastic SOIC (Gull-Wing)
- **E**: Plastic SOJ (J-Lead)
- **F**: Flat Package
- **G**: Plastic DIP Module
- **H**: Plastic SIP Module
- **J**: PLCC
- **L**: Ceramic LCC
- **P**: Plastic DIP
- **S**: Sidebraze DIP
- **X**: Die
- **Z**: Plastic ZIP Module

Speed Designator

Product Designator

Family Designator

- **L**: Logic
- **M**: Memory
- **B**: Module

***Saratoga Semiconductor* Designator**

AMD	SARATOGA
	SSM2148-15
	SSM2148-20
	SSM2148-25
AM2128-35	SSM2148-35
AM2148-45	SSM2148-35
AM2148-55	SSM2148-35
AM2148-70	SSM2148 35
	SSM2149-15
	SSM2149-20
	SSM2149-25
AM2128-35	SSM2149-35
AM2148-45	SSM2149-35
AM2148-55	SSM2149-35
AM2148-70	SSM2149-35
	SSM2150-15
AM9150-20	SSM2150-20
AM9150-25	SSM2150-25
AM9150-35	SSM2150-35
AM9150-45	SSM2150-35
	SSM6167-20
	SSM6167-25
AM2167-35	SSM6167-35
AM2167-45	SSM6167-35
AM2167-55	SSM6167-35
AM2167-70	SSM6167-35
	SSM6168-20
	SSM6168-25
AM2169-40	SSM6168-35
AM2169-50	SSM6168-35
AM2169-70	SSM6168-35
	SSM6168-20
	SSM6168-25
AM2168-40	SSM6168-35
AM2168-50	SSM6168-35
AM2168-#0	SSM6168-35
	SSM6168-20
	SSM6168-25
AM99C68-45	SSM6168-35
AM99C68-55	SSM6168-35
AM99C68-70	SSM6168-35
	SSM7166
	SSM7166-25
AM99C165-35	SSM7166-35
AM99C165-45	SSM7166-35
AM99C165-55	SSM7166-35
AM99C165-70	SSM7166-35
	SSM7188-20
	SSM7188-25
AM99C164-35	SSM7188-35
AM99C164-45	SSM7188-35
AM99C164-55	SSM7188-35
AM99C164-70	SSM7188-35
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	SSL7200A-25
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67C4500-50	SSL7200A-50
67C4500-65	SSL7200A-50
67C4500-80	SSL7200A-50
	SSL7201A-15
	SSL7201A-25
67C4501-35	SSL7201A-35
67C4501-50	SSL7201A-50
67C4501-65	SSL7201A-50
67C4501-80	SSL7201A-50
	SSL7202A-15
	SSL7202A-25
67C4502-35	SSL7202A-35
67C4502-50	SSL7202A-50
67C4502-65	SSL7202A-50
67C4502-80	SSL7202A-50
	SSL7203A-15
	SSL7203A-25
67C4503-35	SSL7203A-35
67C4503-50	SSL7203A-50
67C4503-65	SSL7203A-50
67C4503-80	SSL7203A-50
	SSL7401S-50
67401B	SSL7401S-40
C67401B	SSL7401-25
C67401A	SSL7401-15
C67401	SSL7401 10
	SSL7401-25
67C401-15	SSL7401-15
67C401-10	SSL7401-10
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C67402A	SSL7402-15
C67402	SSL7402-10
	SSL7402-25
67C402-15	SSL7402-15
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	SSL7403S-40
	SSL7403-25
67C4013-15	SSL7403-15
67C4013-10	SSL7403-10
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	SSL7404S-40
	SSL7404-25
67C4023 15	SSL7404-15
67C4023-10	SSL7404-10
	SSL7413S-50
	SSL7413S-40
	SSL7413S 35
	SSL7413-25
67C4033-15	SSL7413 15
67C4033-10	SSL7413-15
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AM10470SA	SSM10470-15
AM10470A	SSM10470-15
	SSM10474-08
AM10474-10	SSM10474-10
AM10474-15	SSM10474-15
AM10474-25	SSM10474-15
	SSM10480-10
AM10480-15	SSM10480-15
AM10480-25	SSM10480-15
	SSM100470-10
AM100470SA	SSM100470-15
AM100470A	SSM100470-15
	SSM100474-08
AM100474-10	SSM100474-10
AM100474 15	SSM100474-15
AM100474 25	SSM100474-15
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AM100480-15	SSM100480-15
AM100480-25	SSM100480-15

CYPRESS	SARATOGA
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CY2148-35	SSM2148-25
CY2148-45	SSM2148-25
CY2148 55	SSM2148-25
	SSM2148-15
	SSM2148-20
CY7C148-25	SSM2148-25
CY7C148-35	SSM2148-25
CY7C148-45	SSM2148-25
	SSM2149-15
	SSM2149-20
CY2149-35	SSM2149-25
CY2149-45	SSM2149-25
CY2149-55	SSM2149-25
	SSM2149 15
	SSM2149 20
CY7C149-25	SSM2149-25
CY7C149-35	SSM2149-25
CY7C149-45	SSM2149-25
CY7C150-15	SSM2150-15
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	SSM2150-20B
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CY7C150-35MB	SSM2150-35B
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CY6116-35	SSM6116-35
CY6116-45	SSM6116-35
CY6116 55	SSM6116-35
	SSM6116-25B
CY6116-35MB	SSM6116-35B
CY6116-45MB	SSM6116-45B
CY6116-55MB	SSM6116-45B
	SSM6116-20
CY7C128-25	SSM6116-25
CY7C128-35	SSM6116-35
CY7C128-45	SSM6116-35
CY7C128 55	SSM6116-35
CY7C128-25MB	SSM6116-25B
CY7C128 35MB	SSM6116-35B
CY7C128 45MB	SSM6116-45B
CY7C128-55MB	SSM6116-45B
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CY7C167-25	SSM6167-25
CY7C167-35	SSM6167-35
CY7C167-45	SSM6167-35
	SSM6168-20
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	SSM6170-20
CY7C170-25	SSM6170-25
CY7C170-35	SSM6170-35
CY7C170-45	SSM6170-35
	SSM6171-20
CY7C171-25	SSM6171-25
CY7C171-35	SSM6171-35
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	SSM6171-25B
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CY7C171-45MB	SSM6171-45B
	SSM6172-20
CY7C172-25	SSM6172-25

CY7C172-35	SSM6172-35
CY7C172-45	SSM6172-35
	SSM6172-25B
CY7C172-35MB	SSM6172-35B
CY7C172-45MB	SSM6172-45B
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CY7C185-55	SSM7164-35
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CY7C185 45MB	SSM7164-45B
CY7C185-55MB	SSM7164-45B
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	SSM7166-25B
CY7C166-35MB	SSM7166-35B
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CY7C164-35	SSM7188-35
CY7C164-45	SSM7188-35
	SSM7188-25B
CY7C164-35MB	SSM7188-35B
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	SSL7203A-15
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CY7C401-10	SSL7401-10
CY7C401-05	SSL7401-10
	SSL7402S-50
	SSL7402S-40
CY7C402-25	SSL7402-25
CY7C402-15	SSL7402-15
CY7C402-10	SSL7402-10
CY7C402-05	SSL7402-10
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MB8416A 15	SSM6116-35
MB8416A-25	SSM6116-35
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	SSM6116-25
MB8417-20	SSM6116-35
MB8417A-12	SSM6116-35
MB8417A-15	SSM6116-35
	SSM6167-20
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MB81C67-45	SSM6167-35
MB81C67-45-W	SSM6167-35
MB81C67-55-W	SSM6167-35
MB8167A-55-W	SSM6167-35
MB8167A 70-W	SSM6167-35
	SSM6168-20
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MB81C68A-35	SSM6168-35
MB81C68A-35	SSM6168-35
MB81C68-45	SSM6168-35
MB81C68-45-W	SSM6168-35
MB81C68 55 W	SSM6168-35
MB8168-55	SSM6168-35
MB8168-70	SSM6168-35
	SSM6168-20
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MB81C69A-30	SSM6168-25
MB81C69A-35	SSM6168-35
	SSM7164-20
	SSM7164-25
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MB8464-70LL	SSM7164-35
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MB81C74-35	SSM7188-35
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	SSM100480-10
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MBM100484-15	SSM100484-15
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HITACHI	SARATOGA
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HM6716-35	SSM6116-35
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HM6267 25	SSM6167-25
HM6267-35	SSM6167-35
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HM6268-25	SSM6168-25
HM6268 35	SSM6168-35
	SSM7164-20
	SSM7164-25
HM6264ASP-10	SSM7164-35
HM6264ASP-12	SSM7164-35
HM6264ASP-15	SSM7164-35
	SSM7166-20
HM6789JP-25	SSM7166-25
HM6789JP 35	SSM7166-35
	SSM7188-20
HM6288P-25	SSM7188-25
HM6288P-35	SSM7188-35
HM6288P-45	SSM7188-35
	SSM7188-20
HM6288LP-25	SSM7188-25
HM6288LP-35	SSM7188-35
HM6288LP-45	SSM7188-35
HM6788P-25	SSM7188 25
HM6788P-35	SSM7188-35
HM6788HP-20	SSM7188-20
HM10470-10	SSM10470-10
HM10470-1	SSM10470-15
HM10470 20	SSM10470-15
	SSM10470 08
HM10474-10	SSM10474-10
HM10474-25	SSM10474-15
	SSM10480-10
HM10480-15	SSM10480-15

HM10480-25	SSM10480-15
HM10484-10	SSM10484-10
	SSM100470-10
HM100470-2	SSM100470-15
HM100474-08	SSM100474-08
HM100474-10	SSM100474-10
HM100474-25	SSM100474-15
	SSM100480-10
HM100480-15	SSM100480-15
HM100484-10	SSM100484-10

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IDT6116SA35TP	SSM6116-35
IDT6116SA45TP	SSM6116-35
IDT6116SA25TDB	SSM6116-25B
IDT6116SA30TDB	SSM6116-25B
IDT6116SA35TDB	SSM6116-35B
IDT6116SA45TDB	SSM6116-45B
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IDT71681SA45P	SSM6171-35
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IDT71681SA45DB	SSM6171-45B
IDT71681SA55DB	SSM6171-45B
IDT71681SA70DB	SSM6171-45B
IDT71681SA85DB	SSM6171-45B
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IDT71682SA45P	SSM6172-35
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IDT71682SA85DB	SSM6172-45B
IDT71682SA100DB	SSM6172-45B
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IDT71691S30P	SSM7161-25
IDT71691S45P	SSM7161-35
IDT71691S35P	SSM7161-35
IDT71691S25DB	SSM7161-25B
IDT71691S30DB	SSM7161-25B
IDT71691S35DB	SSM7161-35B
IDT71691S45DB	SSM7161-45B
IDT71691S55DB	SSM7161-45B
IDT71691S70DB	SSM7161-45B
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IDT71692S30P	SSM7162-25
IDT71692S45P	SSM7162-35
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IDT71692S35DB	SSM7162-35B
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	SSM7164-20
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IDT7164S35P	SSM7164-35
IDT7164S45P	SSM7164-35
	SSM7164-25B
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IDT7164S45DB	SSM7164-45B
IDT67164S55DB	SSM7164-45B
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IDT7164S85DB	SSM7164-45B
IDT7164SIOODB	SSM7164-45B
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IDT7164S150DB	SSM7164-45B
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IDT6198S25P	SSM7166-25
IDT6198S30P	SSM7166-25
IDT6198S45P	SSM7166-35
IDT6198S35P	SSM7166-35
IDT6198S25DB	SSM7166-25B
IDT6198S30DB	SSM7166-25B
IDT6198S35DB	SSM7166-35B
IDT6198S45DB	SSM7166-45B
IDT6198S55DB	SSM7166-45B
IDT6198S70DB	SSM7166-45B
IDT6198S85DB	SSM7166-45B
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IDT7188S25P	SSM7188-25
IDT7188S30P	SSM7188-25
IDT7188S35P	SSM7188-35
IDT7188S45P	SSM7188-35
IDT7188S25DB	SSM7188-25B
IDT7188S30DB	SSM7188-25B
IDT7188S35DB	SSM7188-35B
IDT7188S45DB	SSM7188-45B
IDT7188S55DB	SSM7188-45B
IDT7188S70DB	SSM7188-45B
IDT7188S85DB	SSM7188-45B
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IDT7198S25P	SSM7198-25
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IDT7198S45P	SSM7198-35
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	SSL7201A-15
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	SSL7203A-35
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IDT7203S-80	SSL7203A-50
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IDT72401L-15	SSL7401-15
IDT72401L-10	SSL7401-10
IDT72402L-45	SSL7402S 50
IDT72402L-35	SSL7402S-40
IDT72402L-25	SSL7402-25
IDT72402L-15	SSL77402-15
IDT72402L-IO	SSL7402-10
IDT72403L-45	SSL?403S-50
IDT72403L-35	SSL7403S-40
IDT72403L 25	SSL7403-25
IDT72403L-15	SSL7403-15
IDT72403L-10	SSL7403-10
IDT72404L-45	SSL7404S-50
IDT72404L-35	SSL7404S-40
IDT72404L-25	SSL7404-25
IDT72404L-15	SSL7404-15
IDT72404L-10	SSL7404-10
IDT72413-L45	SSL7413S-50
	SSL7413S-40
IDT72413-L35	SSL7413S-35
IDT72413-L25	SSL7413-25

INMOS	SARATOGA
	SSM2148-15
	SSM2148-20
IMS1223P-25	SSM2148-25
IMS1223P-35	SSM2148-25
IMS1223P-45	SSM2148-25
	SSM2149-15
	SSM2149-20
IMS1223P-25	SSM2149-25
IMS1223P-35	SSM2149-25
IMS1223P-45	SSM2149-25
	SSM6116-20
	SSM6116-25
IMS1433S-35	SSM6116-35
IMS1433S-45	SSM6116-35
IMS1433S-55	SSM6116-35
	SSM6116-25B
IMS1433S-35M	SSM6116-35B

IMS1433S-55M	SSM6116-45B
IMS1433S-70M	SSM6116-45B
	SSM6167-20
IMS1403P-25	SSM6167-25
IMS1403P-35	SSM6167-35
IMS1403P-45	SSM6167-35
IMS1403P-55	SSM6167-35
	SSM6167-20
IMS1403S-25	SSM6167-25
IMS1403S-35	SSM6167-35
IMS1403S-45	SSM6167-35
IMS1403S-55	SSM6167-35
	SSM6168-20
IMS1423P-25	SSM6168-25
IMS1423P-35	SSM6168-35
IMS1423P-45	SSM6168-35
IMS1423P-55	SSM6168-35
	SSM6168-20
IMS1423S-25	SSM6168-25
IMS1423S-35	SSM6168-35
IMS1423S-45	SSM6168-35
IMS1423S-55	SSM6168 35
	SSM7164-20
IMS1630P-25	SSM7164-25
IMS1630P-35	SSM7164-35
IMS1630P-45	SSM7164-35
IMS1630P-55	SSM7164-35
	SSM7164-20
IMS1630S-25	SSM7164-25
IMS1630S-35	SSM7164-35
IMS1630S-45	SSM7164-35
IMS1630S-55	SSM7164-35
	SSM7164-25B
	SSM7164-35B
IMS1630M-45	SSM7164-45B
IMS1630M-55	SSM7164-45B
IMS1630M-70	SSM7164-45B
	SSM7166-20
	SSM7166-25
IMS1624P-35	SSM7166-35
IMS1624P-45	SSM7166-35
IMS1624P-55	SSM7166-35
	SSM7166-20
	SSM7166-25
IMS1624S-35	SSM7166-35
IMS1624S-45	SSM7166-35
IMS1624S-55	SSM7166-35
	SSM7166-25B
	SSM7166-35B
IMS1624S-45M	SSM7166-45B
IMS1624S-55M	SSM7166 45B
IMS1624S-70M	SSM7166-45B
	SSM7188-20
	SSM7188-25
IMS1620P-35	SSM7188-35
IMS1620P-45	SSM7188-35
IMS1620P-55	SSM7188-35
	SSM7188-20
	SSM7188-25
IMS1620S-35	SSM7188 35
IMS1620S-45	SSM7188-35
IMS1620S-55	SSM7188-35
	SSM7188-20
	SSM7188-25
IMS1620Ap-25	SSM7188-35
IMS1620Ap-35	SSM7188-35
	SSM7188-20
	SSM7188-25
IMS1620AS-25	SSM7188-35
IMS1620AS-35	SSM7188-35
	SSM7188-25B
IMS1620S-45M	SSM7188-35B
IMS1620S-55M	SSM7188-45B
IMS1620S-70M	SSM7188-45B

MITSUBISHI SARATOGA

	SSM6167-20
	SSM6167-25
M5M21C68p-35	SSM6167-35
M5M21C68P-45	SSM6167-35
M5M21C68P-55	SSM6167-35
	SSM6168-20
	SSM6168-25
M5M21C68P-35	SSM6168-35
M5M21C68P-45	SSM6168-35
M5M21C68P-55	SSM6168-35
	SSM7164-20
	SSM7164-25
M5M5178P-35	SSM7164-35
M5M5178P-45	SSM7164-35
M5M5178P 55	SSM7164-35
	SSM7188-20
	SSM7188-25
M5M5188P-35	SSM7188-35
M5M5188P-45	SSM7188-35
	SSM7188-20
M5M5188AP-25	SSM7188-25
M5M5188AP-35	SSM7188-35
	SSM10747-08
M10474S-10	SSM10747-10
M10474S-15	SSM10747-15

MOSTEK SARATOGA

	SSL4180-15
MK41H80N-20	SSL4180-20
MK41H80N-25	SSL4180-25
MK41H80N-35	SSL4180-35
	SSL4180-15
MK41H80P 20	SSL4180-20
MK41H80p-25	SSL4180-25
MK41H80p-35	SSL4180-35
MK41H66N-20	SSM6167-20
MK41H66N-25	SSM6167-25
MK41H66N-35	SSM6167-35
MK41H66p-20	SSM6167-20
MK41H66p-25	SSM6167-25
MK41H66p-35	SSM6167-35
MK41H69N-20	SSM6168-20
MK41H69N-25	SSM6168-25
MK41H69N-35	SSM6168-35
MK41H69p-20	SSM6168-20
MK41H69p-25	SSM6168-25
MK41H69P-35	SSM6168-35
MK41H78N-20	SSM6170-20
MK41H78N 25	SSM6170-25
MK41H78N-35	SSM6170-35
MK41H78p-20	SSM6170-20
MK41H78p-25	SSM6170-25
MK41H78p.35	SSM6170-35
	SSL7203A-15
	SSL7203A-25
	SSL7203A-35
MK4503 50	SSL7203A-50
MK4503-65	SSL7203A 50
MK4503-80	SSL7203A-50
MK4503-10	SSL7203A-50

MOTOROLA SARATOGA

	SSL4180-15
MCM4180-22	SSL4180-20
MCM4180-25	SSL4180-25
MCM4180-35	SSL4180-35
MCM2016H-45	SSM6116-35
MCM2016H-55	SSM6116-35
MCM2016H-70	SSM6116-35
	SSM6116-20
	SSM6116-25
MCM2018-35	SSM6116-35
MCM2018-45	SM6116-35
MCM1423-40	SSM6168-35
MCM6268-25	SSM6168-25
MCM6268-35	SSM6168-35
MCM6269-25	SSM6168-25
MCM6269 35	SSM6168-35
	SSM7164-20
	SSM7164-25
MCM6264p-35	SSM7164-35
MCM6264P-45	SSM7164-35
	SSM7166-20
MCM6290P-25	SSM7166-25
MCM6290P-30	SSM7166-25
MCM6290P-35	SSM7166-35
	SSM7188-20
MCM6288P-25	SSM7188-25
MCM6288P-30	SSM7188-25
MCM6288P-35	SSM7188-35
	SSM7188-25B
MCM6288-35BR	SSM7188-35B
MCM6288-45BR	SSM7188-45B

NEC SARATOGA

	SSM6167-20
	SSM6167-25
	SSM6167-35
UPD4311C-35	SSM6167-35
UpD4311C-45	SSM6167-35
UPD4311C-55	SSM6167-35
	SSM6168-20
	SSM6168-25
UPD4314C-35	SSM6168-35
UPD4314C-45	SSM6168-35
UPD4314C-55	SSM6168-35
	SSM7188-20
	SSM7188-25
	SSM7188-35
UPD4362C-45	SSM7188-35
UPD4362C-55	SSM7188-35
UPD10470D10	SSM10470-10
UPD10470D15	SSM10470-15

UPD10474D08	SSM10474-08
UPD10474D10	SSM10474-10
UPD10474D15	SSM10474-15
UPD10480D10	SSM10480-10
UPD10480D15	SSM10480-15
UPD10484D10	SSM10484-10
UPD10484D15	SSM10484-15
UPD100470D10	SSM100470-10
UPD100470D15	SSM100470-15
UPD100474D08	SSM100474-08
UPD100474D10	SSM100474-10
UPD100474D15	SSM100474-15
UPD100480D10	SSM100480-10
UPD100480D15	SSM100480-15
UPD100484D10	SSM100484-10
UPD100484D15	SSM100484-15

PERFORMANCE SARATOGA

P4C148-15PC	SSM2148-15
P4C148-20PC	SSM2148-20
P4C148-25PC	SSM2148-25
P4C148L-15PC	SSM2148-15
P4C148L-20PC	SSM2148-20
P4C148L-25PC	SSM2148-25
P4C149-15PC	SSM2149-15
P4C149-20PC	SSM2149-20
P4C149-25PC	SSM2149-25
P4C149L-15PC	SSM2149-15
P4C149L-20PC	SSM2149-20
P4C149L-25PC	SSM2149 25
P4C150-15PC	SSM2150-15
P4C150-20PC	SSM2150-20
P4C150-25PC	SSM2150-25
P4C150L-15PC	SSM2150-15
P4C150L-20PC	SSM2150-20
P4C150L-25PC	SSM2150-25
P4C116-20PC	SSM6116-20
P4C116-25PC	SSM6116-25
P4C116-30PC	SSM6116-25
P4C116-35PC	SSM6116-35
P4C116-25DMB	SSM6116-25B
P4C116-30DMB	SSM6116-25B
P4C116-35DMB	SSM6116-35B
P4C116-45DMB	SSM6116-45B
P4C168-20PC	SSM6168-20
P4C168-25PC	SSM6168-25
P4C168-30PC	SSM6168-25
P4C168-35PC	SSM6168-35
P4C168L-20PC	SSM6168-20
P4C168L-25PC	SSM6168-25
P4C168L-30PC	SSM6168-25
P4C168L-35PC	SSM6168-35
P4C169-20PC	SSM6168-20
P4C169-25PC	SSM6168-25
P4C169-30PC	SSM6168-25
P4C169-35PC	SSM6168-35
P4C170-20PC	SSM6170-20
P4C170-25PC	SSM6170-25
P4C170-30PC	SSM6170-25
P4C1681-20PC	SSM6171-20
P4C1681-25PC	SSM6171-25
P4C1681-30PC	SSM6171-25
P4C1681-35PC	SSM6171-35
P4C1681-25DMB	SSM6171-25B
P4C1681-30DMB	SSM6171-25B
P4C1681-35DMB	SSM6171-35B
P4C1681-45DMB	SSM6171-45B
P4C1681L-20PC	SSM6171-20
P4C1681L-25PC	SSM6171-25
P4C1681L-30PC	SSM6171-25
P4C1681L-35PC	SSM6171-35
P4C1681L-25DMS	SSM6171-25B
P4C1681L-30DMB	SSM6171-25B
P4C1681L-35DMB	SSM6171-35B
P4C1681L-45DMB	SSM6171-45B
P4C1682-20PC	SSM6172-20
P4C1682-25PC	SSM6172-25
P4C1682-30PC	SSM6172-25
P4C1682-35PC	SSM6172 35
P4C1682-25DMB	SSM6172-25B
P4C1682-30DMB	SSM6172-25B
P4C1682-35DMB	SSM6172-35B
P4C1682-45DMB	SSM6172-45B
P4C1682L-20PC	SSM6172-20
P4C1682L-25PC	SSM6172-25
P4C1682L-30PC	SSM6172-25
P4C1682L-35PC	SSM6172-35
P4C1682L-25DMB	SSM6172-25B
P4C1682L-30DMB	SSM6172-25B
P4C1682L-35DM	SSM6172-35B
P4C1682L-45DMB	SSM6172-45B
P4C164-20PC	SSM7164-20
P4C164-25PC	SSM7164-25
P4C164-30PC	SSM7164-25
P4C164-35pC	SSM7164-35
P4C164-25CMB	SSM7164-25B
P4C164-30CMB	SSM7164-25B
P4C164-35CMB	SSM7164-35B
P4C164-45CMB	SSM7164-45B
P4C164-55CMB	SSM7164-45B
P4C164L-20PC	SSM7164-20
P4C164L-25PC	SSM7164-25
P4C164L-30PC	SSM7164-25
P4C164L-35PC	SSM7164-35
P4C164L-25CMB	SSM7164-25B
P4C164L-30CMB	SSM7164-25B
P4C164L-35CMB	SSM7164-35B
P4C164L-45CMB	SSM7164-45B
P4C164L-55CMB	SSM7164-45B
P4C198-20PC	SSM7166-20
P4C198-25PC	SSM7166-25
P4C198-30PC	SSM7166-25
P4C198-35PC	SSM7166-35
P4C198-25CMB	SSM7166-25B
P4C198-30CMB	SSM7166-25B
P4C198-35CMB	SSM7166-35B
P4C198-45CMB	SSM7166-45B
P4C198 55CMB	SSM7166-45B
P4C198L-20PC	SSM7166-20
P4C198L-25PC	SSM7166-25
P4C198L-35PC	SSM7166-35
P4C198L-30PC	SSM7166-25
P4C198L-25CMB	SSM7166-25B
P4C198L-30CMB	SSM7166-25B
P4C198L-35CMB	SSM7166-35B
P4C198L-45CMB	SSM7166-45B
P4C198L-55CMB	SSM7166-45B
P4C188-20PC	SSM7188-20
P4C188-25PC	SSM7188-25
P4C188-30PC	SSM7188-25
P4C188-35PC	SSM7188-35
P4C188-25CMB	SSM7188 25B
P4C188-30CMB	SSM7188-25B
P4C188-35CMB	SSM7188-35B
P4C188-45CMB	SSM7188-45B
P4C188-55CMB	SSM7188-45B
P4C188L-20PC	SSM7188-20
P4C188L-25PC	SSM7188-25
P4C188L-30PC	SSM7188-25
P4C188L 35PC	SSM7188-35
P4C188L-25CMB	SSM7188-25B
P4C188L-30CMB	SSM7188-25B
P4C198A 20PC	SSM7198-20
P4C198A-25PC	SSM7198-25
P4C198A-30PC	SSM7198-25
P4C198A-35PC	SSM7198-35
P4C198A-25CMB	SSM7198-25B
P4C198A-30CMB	SSM7198-25B
P4C198A-35CMB	SSM7198-35B
P4C198A-45CMB	SSM7198-45B
P4C198A 55CMB	SSM7198-45B
P4C198AL-20PC	SSM7198-20
P4C198AL-25PC	SSM7198-25
P4C198AL-35PC	SSM7198-35
P4C198AL-30PC	SSM7198-25
P4C198AL-25CMB	SSM7198-25B
P4C198AL-30CMB	SSM7198-25B
P4C198AL-35CMB	SSM7198-35B
P4C198AL-45CMB	SSM7198-45B
P4C198AL-55CMB	SSM7198-45B

TI SARATOGA

	SSL2152-20
TACT2152-25	SSL2152-25
TACT2152-30	SSL2152-30
TACT2152-35	SSL2152-30
	SSL2154-20
TACT2154-25	SSL2154-25
TACT2154-30	SSL2154-30
TACT2154-35	SSL2154-30

TOSHIBA SARATOGA

	SSM6116-20
TMM2018AP-25	SSM6116-25
TMM2018AP-35	SSM6116-35
TMM2018AP-45	SSM6116-35
	SSM6168-20
TMM2068-25	SSM6168-25
TMM2068 35	SSM6168-35
TMM2068-45	SSM6168-35
	SSM7164-20
	SSM7164-25
TMM2088-35	SSM7164-35
TMM2088-45	SSM7164-35
TC5588P-20	SSM7164-20
TC5588P-25	SSM7164-25
TC5588P-35	SSM7164-35
	SSM7166-20
TC55417P-25	SSM7166-25
TC55417P-35	SSM7166-35
	SSM7188-20
TC55416P-25	SSM7188-25

QUALITY AND RELIABILITY

THE CORPORATE QUALITY COMMITMENT

It is Saratoga's intent to provide products and service in a timely manner and at a competitive cost without compromising quality. In order to ensure maximum customer satisfaction, it is the policy of Saratoga to analyze customer requirements on a one for one basis at the earliest practical stage of the contract. This includes planning with respect to requirements, resources, systems and procedures.

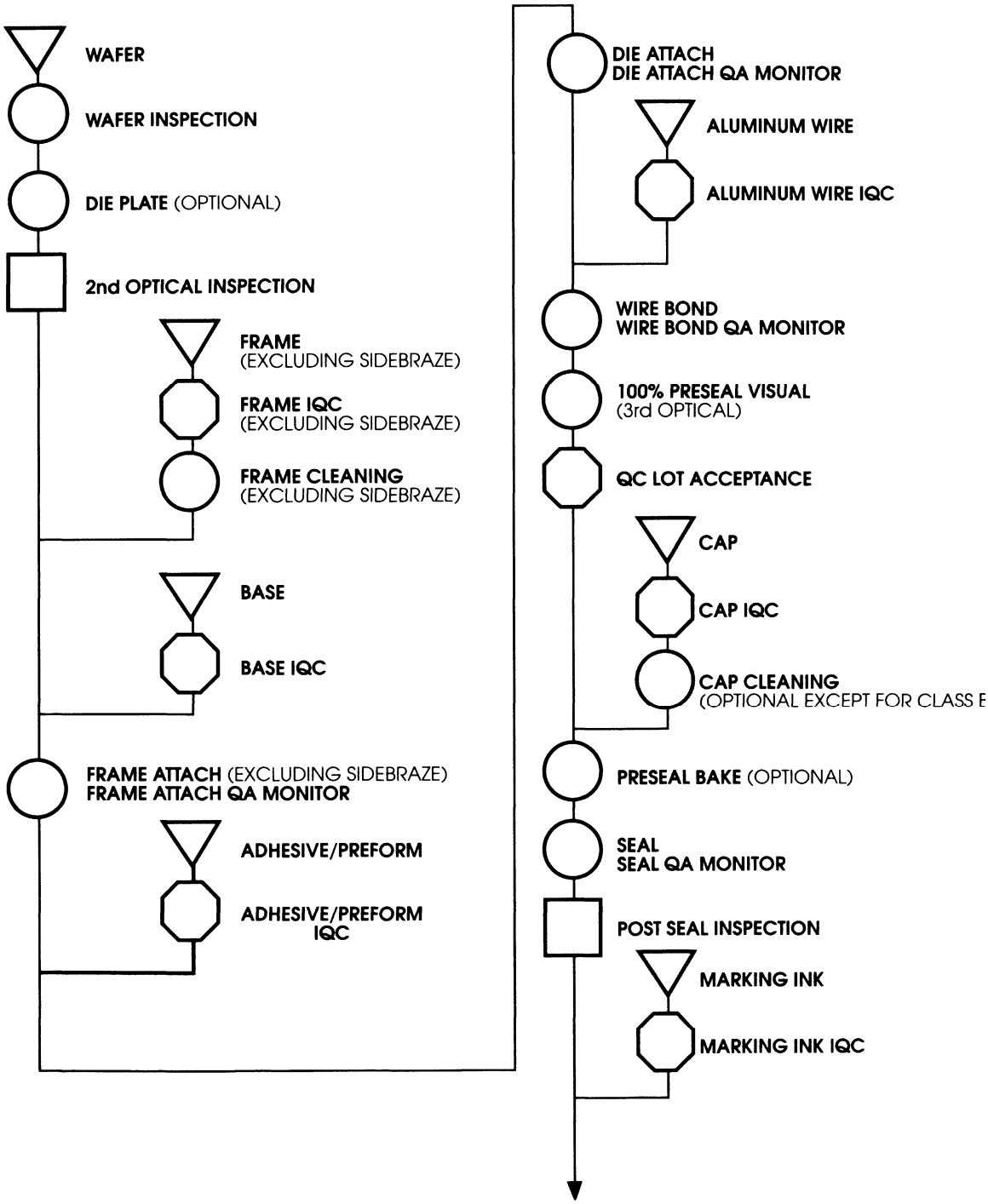
The Quality Assurance Program Plan includes, but is not limited to, the following areas:

- **DESIGN**
- **MATERIAL PROCUREMENT**
- **MATERIAL CONTROL**
- **ELECRONIC TEST**
- **ENVIRONMENTAL TEST**
- **ASSEMBLY**
- **INSPECTION**
- **STORAGE**
- **PACKING**
- **SHIPMENT**
- **WORK INSTRUCTIONS**
- **RECORDS**
- **MAINTENANCE**
- **CALIBRATION**
- **CORRECTIVE ACTION**

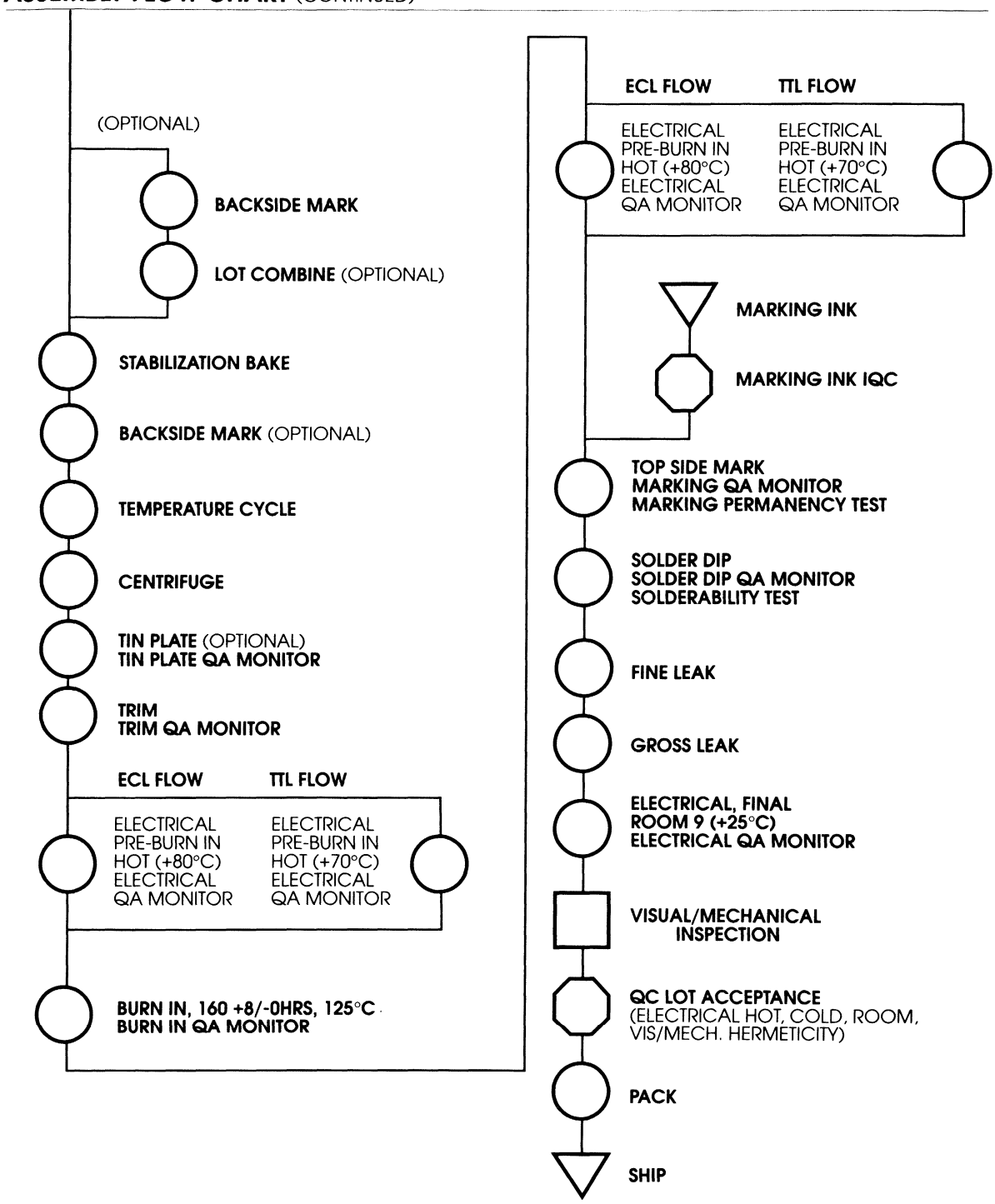
For more details in the above areas, write or call for the Saratoga Quality Assurance Policy Manual.

The production flow that Saratoga has chosen for manufacturing and testing standard product meets, or exceeds, the requirements for military compliant products. The intent is to build at the wafer FAB level, apply stringent testing and inspection throughout the assembly process, and ensure the highest level of quality and reliability. Refer to the following assembly flow chart for a detailed look at Saratoga's testing and inspection methodology.

ASSEMBLY FLOW CHART



ASSEMBLY FLOW CHART (CONTINUED)



THE CORPORATE RELIABILITY COMMITMENT

The Reliability plan is implemented when a design is turned into working silicon. This plan includes qualification, monitor, failure anaysis and data collection. All testing is done in accordance with the applicable methods of MIL-STD-883.

The Qualification program includes new device designs, process technologies, package designs, and subcontractors.

The Monitor program is designed to carry out Saratoga's commitment to reliability. The levels of stress applied are defined in Method 5005, Group C and D of MIL-STD-883. The following table shows these levels.

Failure analysis is performed , as applicable, and all relevant data is fed back into the system for product/process improvement.

GROUP C TEST	METHOD	CONDITION/COMMENTS
SUBGROUP 1		
(a) Steady State Life Test	1005	184 hrs minimum at 150 °C
(b) End-Point Electrical Parameters		As specified in the applicable device specification.
SUBGROUP 2		
(a) Temperature Cycling	1010	Test Condition C, 10 cycle
(b) Constant Acceleration	2001	Test Condition E, Y1 orientation only.
(c) Seal	1014	
(1) Fine		Test Condition A or B, B perferred.
(2) Gross		Test Condition C.
(d) Visual Examination	1010	Visual criteria only.
(e) End-Point Electrical		As specified in the applicable device specification.

GROUP D TEST	METHOD	CONDITION/COMMENTS
SUBGROUP 1		
(a) Physical Dimensions	2016	
SUBGROUP 2		
(a) Lead Integrity	2004	Test Condition B2 (Lead Fatigue), 15 units, 3 leads per unit.
(b) Seal	1014	Not required for solder sealed packages.
(1) Fine		Test Condition A or B, B perferred.
(2) Gross		Test Condition C.
SUBGROUP 3		
(a) Thermal Shock	1011	Test Condition B, 15 cycles.
(b) Temperature Cycling	1010	Test Condition C, 100 cycles.
(c) Moisture Resistance	1004	
(d) Seal	1014	
(1) Fine		Test Condition A or B, B perferred.
(2) Gross		Test Condition C.
(e) Visual Examination	1010	Visual criteria only.
(f) End-Point Electrical Parameters		As specified in the applicable specification.
SUBGROUP 4		
(a) Mechanical Shock	2002	Test Condition B.
(b) Vibration, Variable Frequency	2007	Test Condition A.
(c) Constant Acceleration	2001	Test Condition E, Y1 orientation only.
(d) Seal	1014	
(1) Fine		Test Condition A or B, B perferred.
(2) Gross		Test Condition A.
(e) Visual Examination	1010	Visual criteria only.
(f) End-Point Electrical Parameters		As specified in the applicable device specification.
SUBGROUP 5		
(a) Salt Atmosphere	1009	Test Condition A.
(b) Seal	1014	
(1) Fine		Test Condition A or B, B perferred.
(2) Gross		Test Condition C.
(c) Visual Examination	1009	Visual criteria only.
SUBGROUP 6		
(a) Internal Water Vapor Content	1018	5,000 ppm max. water content at 100 °C.
SUBGROUP 7		
(a) Adhesion of Lead Finish	2025	Use 5 packages, pick 3 random leads per package.
SUBGROUP 8		
(a) Lid Torque	2024	For Frit or Glass sealed packages only.

THE CORPORATE MILITARY COMMITMENT

The security of our nation today rests heavily on both the quaility of our electronic technology and our commitment to achieving new levels of performance. This has created an urgent need for defense electronics systems to perform flawlessly under adverse conditions.

It is this challenge that Saratoga Semiconductor has accepted, impelling the company to develop a portfolio of military products that meet the high reliability and performance requirements of advanced programs such as the Strategic Defense Initiative. The company sees a broad range of applications for its military products, in areas such as digital signal processing, C^3I, image processing, and other technologies critical to the electronic battlefield.

Founded in 1985, Saratoga semiconductor has become an established designer, manufacturer and marketer of high-performance BiCMOS integrated circuits. The products are intended for customers who require the fastest processing speeds . . . over the full temperature range . . . and lowest power possible from today's state-of-the-art device technology. Saratoga's corporate strategy is product innovation targeted at applications where these performance improvements have the greatest effect.

Saratoga is offering military versions of these products to selected defense industry manufacturers. In addition, the company has a dedicated team of personnel with expertise in defense electronics applications. This team is ready to assist Saratoga customers in meeting their needs for military-screened ICs.

Military grade devices supplied by Saratoga are processed in accordance with MIL-STD-883 Methods 5004 and 5005. The following flow details our commitment to producing Class B military product.

SARATOGA MILITARY CLASS B PRODUCT FLOW

STEP	PROCESSING	MIL-STD 883 TEST METHOD	QC/QA ACTIVITY
1) Customer P.O.	Customer Purchase Order is received and reviewed by QC for specific P.O. requirements.		
2) Order Entry & P.O. Review	P.O. is entered into Saratoga's computerized order-processing system and reviewed internally.		QC Monitor
3) Wafer Fabrication	Wafers are fabricated in Saratoga's Class 10 clean room area, utilizing state-of-the-art processing equipment. Humidity, temperature and particulate contamination levels are strictly controlled.		QC Monitor/ QA Audits
4) Wafer Sort Electrical Test	Individual die are 100% parametrically and functionally tested to the detailed device specifications. Wafers are then cut and separated.		
5) Assembly / Test	Assembly/Test procedures follow:	Based on Method 5004	QC Monitor
Internal Visual	Die are assembled and 100% visually inspected to strict internal criteria.	2010	
Stabilization Bake	100% of sealed products are subjected to thermal/mechanical stress tests, including stabilization bake, temperature cycle, and constant acceleration. These tests are designed to screen out products that exhibit structural or mechanical weaknesses.	1008	
Temperature Cycle		1010	
Constant Acceleration		2001	
Visual 100%	Products are 100% visually inspected for missing leads, broken packages, or lids off.		QC Monitor
Pre Burn-In Electical	100% of the devices are electrically tested to Saratoga data sheet or customer specifications prior to burn-in.		QC Monitor
Burn-In	100% of products are burned in for 160 hours at +125°C.	1015	QC Monitor
Post Burn-In Electrical	After burn-in, 100% of products are electrically tested to Saratoga data sheet or customer specifications.		QC Monitor
PDA Calculation	The percent defective allowable (PDA) is calculated, based on Method 5004.		QC Monitor
Solder Dip Lead Finish	Solder dip (for CERDIP packages) and lead finish steps are completed.		QC Monitor
Fine and Gross Leak	100% of products are screened for hermeticity.	1014	QC Monitor
Final Electrical	100% of products are tested at hot, room and cold temperatures, based on Method 5004.		QC Monitor
Qualification/Quality Conformance	Electrical and visual/mechanical qualification and quality conformance testing is performed.	Based on 5005 Group A & B	QC Monitor
External Visual	100% of products are subjected to an external visual inspection.	2009	QC Monitor
Qualification/ Quality Conformance	Die and package related qualification and quality conformance testing is performed.	Based on 5005 Group C & D	
6) QA Plant Clearance Inspection	Product is subjected to final QA inspection prior to shipment. Certification of conformance is generated and provided.		QC Monitor
7) Shipment	Products are shipped to Saratoga's customer.		

BiCMOS TTL SRAMS

Saratoga Semiconductor

SSM2148/9

4K 1,024 Words by 4 Bits BiCMOS TTL Static RAM

FEATURES

- **Fast Access Times**
  15/20/25ns Commercial Temperature
  15/25/35ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military Temperature Range**
- **Automatic Power Down when Deselected** (SSM2148)
- **Industry Standard 20-Pin DIP & SOJ Packages**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

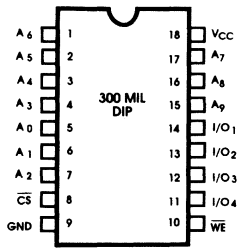
The SSM2148 and SSM2149 are high performance 4K BiCMOS static RAMs organized 1024 words by 4 bits. These devices are targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. They are also designed for use in communication, industrial and military equipment applications.

The high speed (15ns), low active power consumption (50mA) and high output drive (16mA) of the SSM2148 and SSM2149 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are low. Data on the Input/Output pins (I/O_1- I/O_4) is written into the memory cell specified by the 10 bit address placed on the Address Inputs (A_0- A_9). With $\overline{CS}$ low, $\overline{WE}$ high and the Output Enable input transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

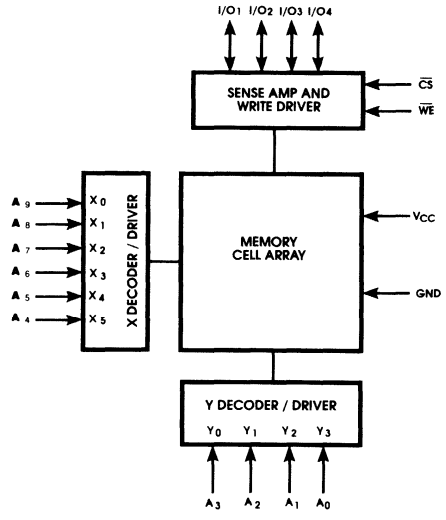
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_9	Address Inputs
I/O_1 - I/O_4	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
V_{CC}	Power Supply Pins
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	I/On	POWER
Read	L	H	DO	ACTIVE
Write '0'	L	L	L	ACTIVE
Write '1'	L	L	H	ACTIVE
Disabled	H	X	HIGH Z	STANDBY (1)

H = High Voltage Level
L = Low Voltage Level
X = Irrelevant
DO = Valid Data Out
X = Irrelevant(1) For SSM2148 only.

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		250	mW
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM2148/9 MIN	SSM2148/9 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		10/25	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

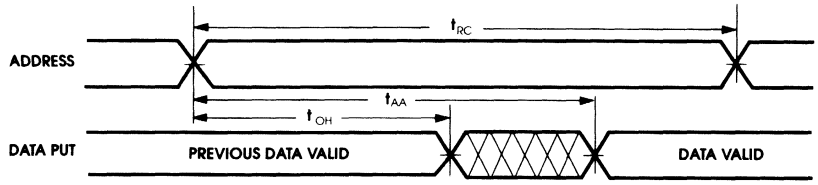
READ CYCLE

PARAMETER	SYMBOL	VALUE				UNIT
		COM SSM2148/9-15	COM/MIL SSM2148/9-20	COM/MIL SSM2148/9-25	MIL SSM2148/9-35	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
Read Cycle Time	t_{RC}	15	20	25	35	ns
Address Access Time	t_{AA}	15	20	25	35	ns
Chip Select Access Time	t_{ACS}	10	15	20	25	ns
Output Hold from Address Change	t_{OH}	3	3	3	3	ns
Chip Selection to Output in LOW Z	t_{LZ}	3	3	3	3	ns
Chip Selection to Output in HIGH Z	t_{HZ}	12	15	20	25	ns
Chip Selection to Power Up Time	t_{PU}[2]	0	0	0	0	ns
Chip Deselection to Power Down Time	t_{PD}[2]	10	15	20	25	ns

[2] These parameters are sampled and not 100% tested.

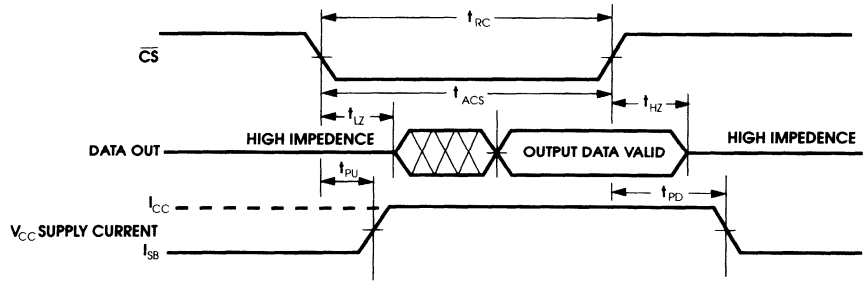
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ is high for Read Cycle. $\overline{CS}$ is low, device is continuously selected. All read Cycle timings are referenced from the last valid address to the first transitioning address.



READ CYCLE TIMING DIAGRAM NO. 2

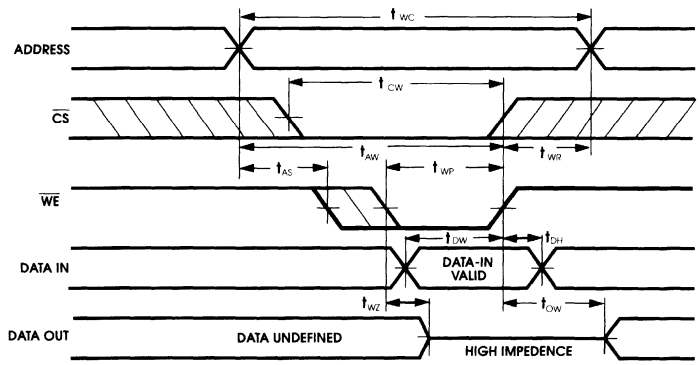
$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.



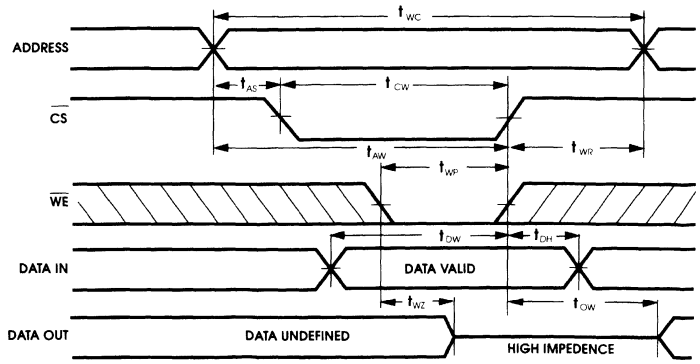
WRITE CYCLE

		VALUE				
		COM SSM2148/9-15	COM/MIL SSM2148/9-20	COM/MIL SSM2148/9-25	MIL SSM2148/9-35	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	15	20	25	35	ns
Chip Selection to End of Write	t_{CW}	15	20	25	35	ns
Address Valid to End of Write	t_{AW}	15	20	25	35	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	15	20	25	35	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	10	12	15	20	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	6	8	10	15	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]



WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

CAPACITANCE

PARAMETER	SYMBOL	TYP VALUE	UNIT
Input Pin Capacitance	C_{IN}	5	pF
Output Pin Capacitance	C_{OUT}	7	pF

AC TEST CONDITIONS

[4] Including scope and jig

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Level	1.5V
Output Load	Figures 1 and 2

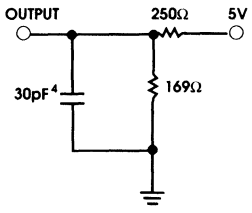


Figure 1

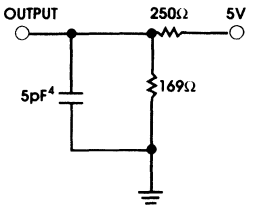
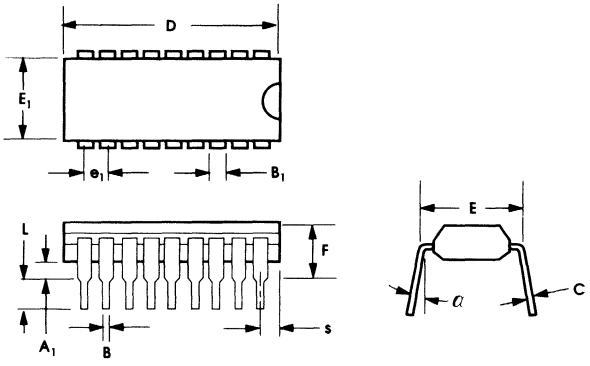


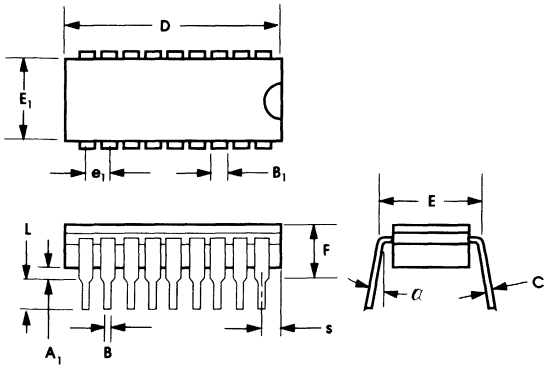
Figure 2

PACKAGE DIMENSIONS



18 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
C	.008	.012
D	.890	.910
E	.280	.300
E_1	.255	.265
e_1	.090	.110
F		.170
L	.125	.135
s	.060	.070
α	0°	15°



18 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.045
B	.014	.023
B_1	.050	.065
C	.009	.015
D		.920
E	.300	.320
E_1	.285	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM2148-15PC SSM2148-20PC SSM2148-25PC	15ns 20 25	18-Pin Plastic DIP	0	+70	°C
SSM2148-15CC SSM2148-20CC SSM2148-25CC	15ns 20 25	18-Pin CERDIP			
SSM2148-15CM SSM2148-20CM SSM2148-25CM SSM2148-35CM	15ns 20 25 35	18-Pin CERDIP	-55	+125	°C
SSM2149-15PC SSM2149-20PC SSM2149-25PC	15ns 20 25	18-Pin Plastic DIP	0	+70	°C
SSM2149-15CC SSM2149-20CC SSM2149-25CC	15ns 20 25	18-Pin CERDIP			
SSM2149-15CM SSM2149-20CM SSM2149-25CM SSM2149-35CM	15ns 20 25 35	18-Pin CERDIP	-55	+125	°C

Saratoga Semiconductor

SSM2150

4K 1,024 Words by 4 Bits BiCMOS TTL Static RAM
with Separate Data Inputs and Outputs

PRELIMINARY INFORMATION

FEATURES

- **Fast Access Times**
  15/20/25/35ns max
- **Separate Data Inputs & Outputs**
- **Full Military 883C Level B.**
- **Fully TTL I/O Compatible**
- **Industry Standard 300 MIL DIP**
- **SABiC BiCMOS Fabrication Technology**
  High Performance - 15ns
  High Output Drive - 16mA

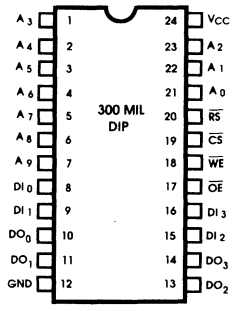
DESCRIPTION

Organized as 1,024 x 4 bits, the SSM2150 is a high-performance 4,096-bit TTL BiCMOS static RAM. This device is targeted for use in the implementation of writeable control store, cache memory and high speed lookup-up table.

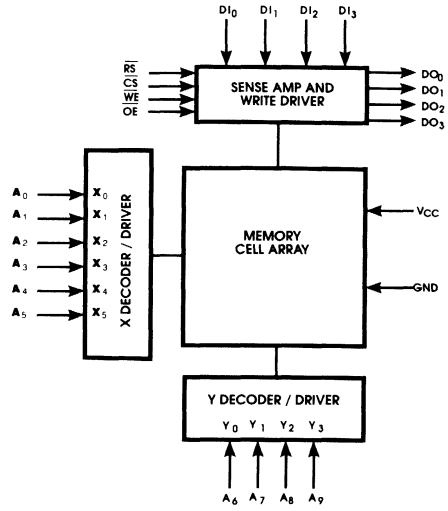
Separate data input and output buses improves performance of the device by avoiding the need to multiplex common data I/O. Outputs are tri-stated during write, reset, deselect, or when output enable ($\overline{OE}$) is held HIGH, allowing for easy memory expansion. Reset is initiated by selecting the devices ($\overline{CS}$ = LOW) and pulsing the reset ($\overline{RS}$) input LOW. Within two memory cycles, all memory cells are reset to zeros. Chip select must be LOW for the device to reset. An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation. When ($\overline{CS}$) and ($\overline{WE}$) are LOW, data on DI_0 to DI_3 is written into the addressed memory location and the output circuitry is preconditioned so that the write data is present at the output at the completion of write cycle. Reading is performed with the chip select ($\overline{CS}$) input LOW, and the write enable ($\overline{WE}$) input HIGH, and the output enable ($\overline{OE}$) LOW. The data stored in the addressed location is read out on the four non-inverting output pins DO_0 to DO_3. The outputs of the memory go to an active high impedance state whenever chip select is HIGH, reset is LOW, output enable is HIGH, or during the writing operation when write enable is LOW.

All inputs are TTL compatible, the SSM2150 offers an output drive of 16mA, which is twice that of conventional CMOS designs.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



July 1988

Saratoga Semiconductor

SSM6167

16K 16,384 Words by 1 Bits BiCMOS TTL Static RAM

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard 20-Pin Package**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

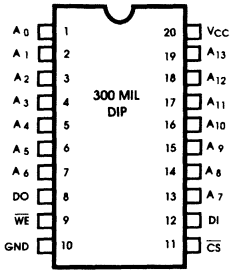
The SSM6167 is a high performance 16K BiCMOS static RAM organized 16,384 words by 1 bit. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power consumption (60mA) and high output drive (16mA) of the SSM6167 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are low. Data on the Data Input (DI) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0- A_{13}). With $\overline{CS}$ low, $\overline{WE}$ high, the content of the addressed memory cell is transferred to Data Output (DO).

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

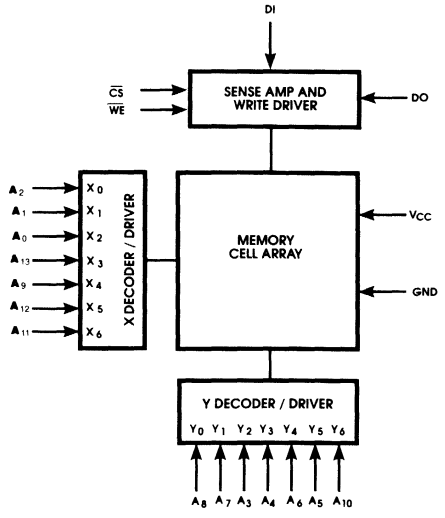
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{13}	Address Inputs
DI	Data Inputs
DO	Data Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
Vcc	Power Supply Pins
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	DI	DO	POWER
Read	L	H	X	DO	ACTIVE
Write '0'	L	L	L	HIGH Z	ACTIVE
Write '1'	L	L	X	HIGH Z	ACTIVE
Disabled	H	X	X	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM6167 MIN	SSM6167 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH} =-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		60	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

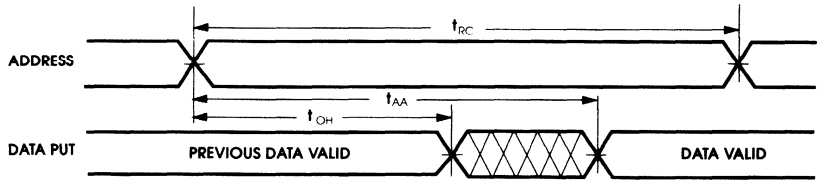
READ CYCLE

PARAMETER	SYMBOL	VALUE				UNIT
		COM SSM6167-20		COM/MIL SSM6167-25		COM/MIL SSM6167-35		MIL SSM6167-45		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	20		25		35		45		ns
Address Access Time	t_{AA}		20		25		35		45	ns
Chip Select Access Time	t_{ACS}		15		20		25		30	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Output in LOW Z	t_{LZ}	3		3		3		3		ns
Chip Selection to Output in HIGH Z	t_{HZ}		15		20		25		30	ns
Chip Selection to Power Up Time	t_{PU}[2]	0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}[2]		15		20		25		30	ns

[2] These parameters are sampled and not 100% tested.

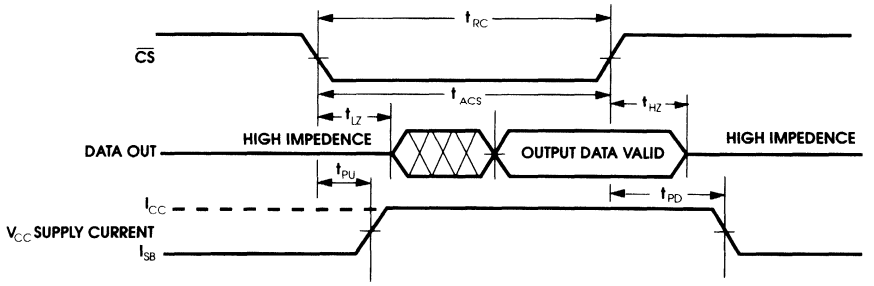
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ is high for Read Cycle. $\overline{CS}$ is low, device is continuously selected. All read Cycle timings are referenced from the last valid address to the first transitioning address.



READ CYCLE TIMING DIAGRAM NO. 2

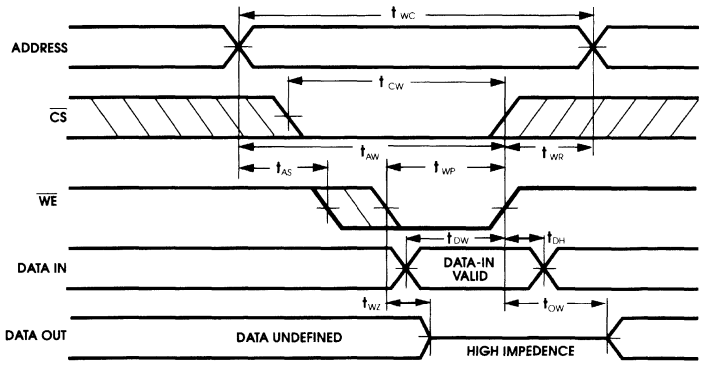
$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.



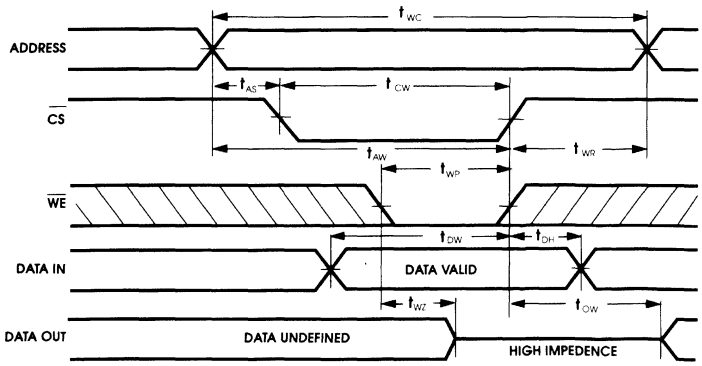
WRITE CYCLE

		VALUE				
		COM SSM6167-20	COM/MIL SSM6167-25	COM/MIL SSM6167-35	MIL SSM6167-45	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	20	25	35	45	ns
Chip Selection to End of Write	t_{CW}	20	25	35	45	ns
Address Valid to End of Write	t_{AW}	20	25	35	45	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	20	25	35	45	ns
Write Recovery Time	t_{WR}	2	0	0	0	ns
Data Valid to End of Write	t_{DW}	12	15	20	25	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	10	15	20	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]



WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



[3] If $\overline{CS}$ goes high simultaneously with WE high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

CAPACITANCE

PARAMETER	SYMBOL	TYP VALUE	UNIT
Input Pin Capacitance	C_{IN}	5	pF
Output Pin Capacitance	C_{OUT}	7	pF

AC TEST CONDITIONS

[4] Including scope and jig

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Level	1.5V
Output Load	Figures 1 and 2

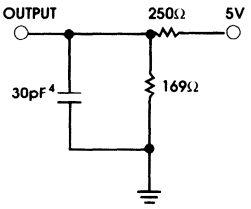


Figure 1

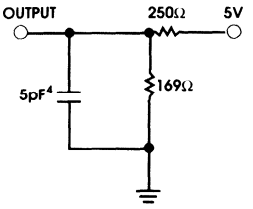
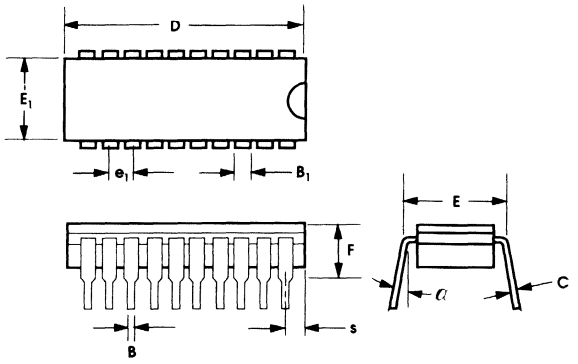


Figure 2

PACKAGE DIMENSIONS



20 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.060
E	.290	.320
E_1	.220	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM6167-20CC SSM6167-25CC SSM6167-35CC	20ns 25ns 35ns	20-Pin CERDIP	0	+70	°C
SSM6167-25CM SSM6167-35CM SSM6167-45CM	25ns 35ns 45ns	20-Pin CERDIP	-55	+125	°C

Saratoga Semiconductor

SSM6168

16K 4,096 Words by 4 Bits BiCMOS TTL Static RAM

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military Temperature Range**
- **Industry Standard 20-Pin DIP & SOJ Packages**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

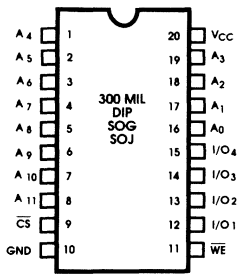
The SSM6168 is a high performance 16K BiCMOS static RAM organized 4096 words by 4 bits. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power consumption (90mA) and high output drive (16mA) of the SSM6168 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are low. Data on the Input/Output pins (I/O_1- I/O_4) is written into the memory cell specified by the 12 bit address placed on the Address Inputs (A_0- A_{11}). With $\overline{CS}$ low, $\overline{WE}$ high and the Output Enable input transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

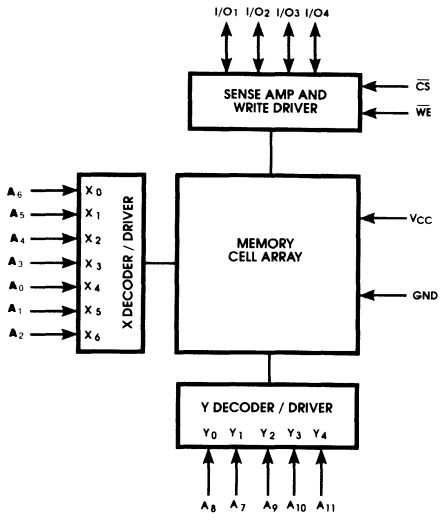
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{11}	Address Inputs
I/O_1 - I/O_4	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
V_{CC}	Power Supply Pins
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	I/On	POWER
Read	L	H	DO	ACTIVE
Write '0'	L	L	L	ACTIVE
Write '1'	L	L	H	ACTIVE
Disabled	H	X	HIGH Z	STANDBY

H = High Voltage Level
L = Low Voltage Level
X = Irrelevant
DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM6168 MIN	SSM6168 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		90	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

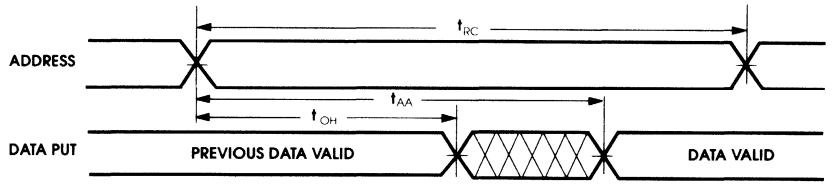
READ CYCLE

PARAMETER	SYMBOL	VALUE								UNIT
		COM SSM6168-20		COM/MIL SSM6168-25		COM/MIL SSM6168-35		MIL SSM6168-45		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	20		25		35		45		ns
Address Access Time	t_{AA}		20		25		35		45	ns
Chip Select Access Time	t_{ACS}		15		20		25		30	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Output in LOW Z	t_{LZ}	3		3		3		3		ns
Chip Selection to Output in HIGH Z	t_{HZ}		15		20		25		30	ns
Chip Selection to Power Up Time	t_{PU}[2]	0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}[2]		15		20		25		30	ns

[2] These parameters are sampled and not 100% tested.

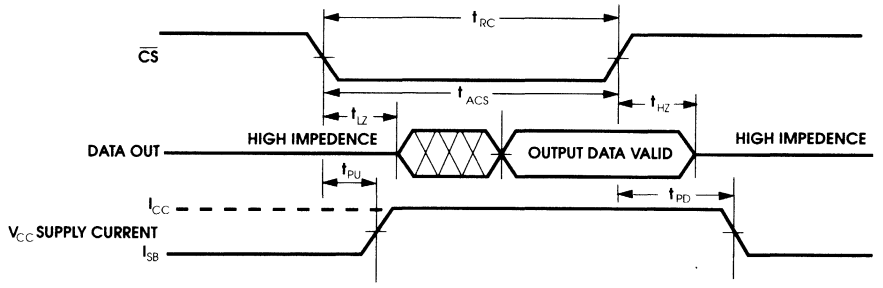
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ is high for Read Cycle. $\overline{CS}$ is low, device is continuously selected. All read Cycle timings are referenced from the last valid address to the first transitioning address.



READ CYCLE TIMING DIAGRAM NO. 2

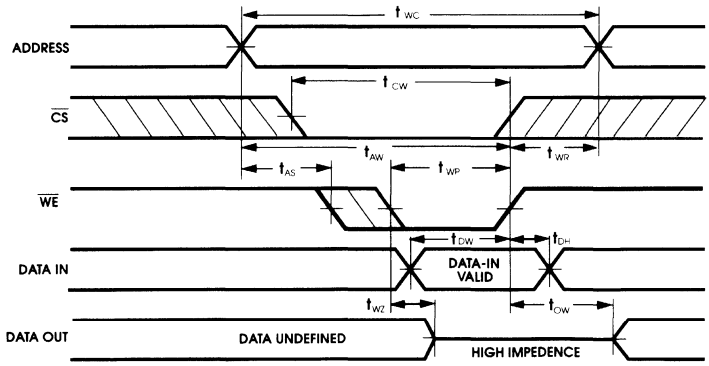
$\overline{WE}$ = V_{IH} , $\overline{OE}$ = V_{IL} . Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.



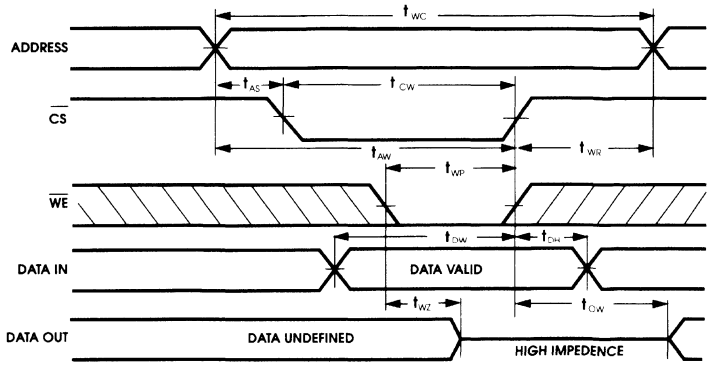
WRITE CYCLE

		VALUE				
		COM SSM6168-20	COM/MIL SSM6168-25	COM/MIL SSM6168-35	MIL SSM6168-45	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	20	25	35	45	ns
Chip Selection to End of Write	t_{CW}	20	25	35	45	ns
Address Valid to End of Write	t_{AW}	20	25	35	45	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	20	25	35	45	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	12	15	20	25	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	10	15	20	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]



WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

CAPACITANCE

PARAMETER	SYMBOL	TYP VALUE	UNIT
Input Pin Capacitance	C_{IN}	5	pF
Output Pin Capacitance	C_{OUT}	7	pF

AC TEST CONDITIONS

[4] Including scope and jig

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Level	1.5V
Output Load	Figures 1 and 2

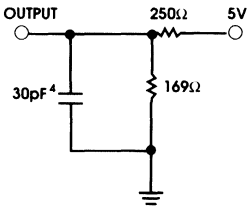


Figure 1

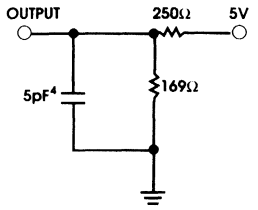
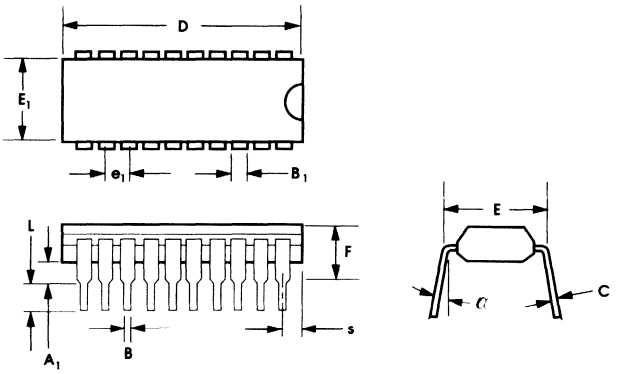


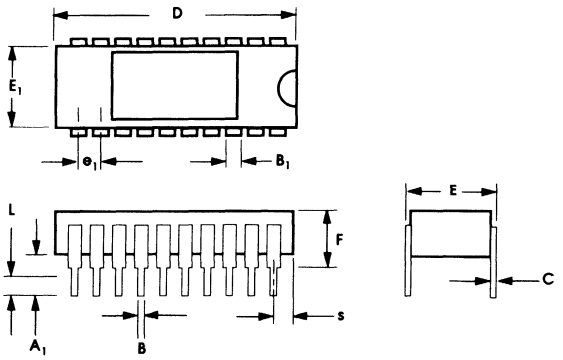
Figure 2

PACKAGE DIMENSIONS



20 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

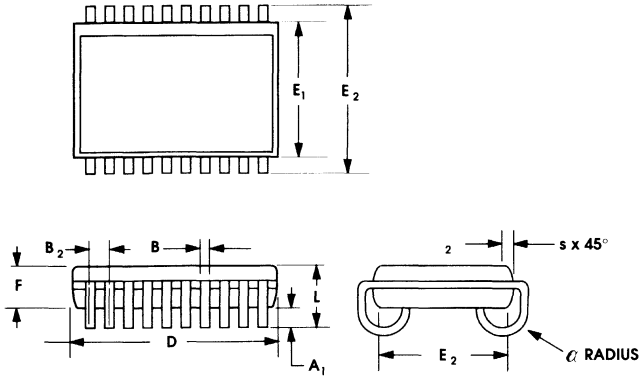
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.065
C	.008	.012
D	1.023	1.033
E	.280	.300
E_1	.245	.255
e_1	.090	.110
F		.170
L	.125	.135
s	.060	.070
α	0°	15°



20 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.060
E	.290	.320
E_1	.220	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080

PACKAGE DIMENSIONS (CONTINUED)



20 LEAD MOLDED SOJ

	INCHES	
PARAMETER	MIN	MAX
A_1	.028	.036
B	.014	.019
B_1	.045	.055
D	.500	.510
E	.335	.347
E_1	.292	.299
E_2	.262	.272
F	.090	.094
L	.120	.140
s	.010	.016
α	.031	.042

ORDERING INFORMATION

			TEMPERATURE RANGE		
PART NUMBER	SPEED	PACKAGE	MIN	MAX	UNIT
SSM6168-20PC SSM6168-25PC SSM6168-35PC	20ns 25ns 35ns	20-Pin Plastic DIP	0	+70	°C
SSM6168-20EC SSM6168-25EC SSM6168-35EC	20ns 25ns 35ns	20-Pin SOJ			
SSM6168-20SC SSM6168-25SC SSM6168-35SC	20ns 25ns 35ns	20-Pin Sidebraze DIP			
SSM6168-25SM SSM6168-35SM SSM6168-45SM	25ns 35ns 45ns	20-Pin Sidebraze DIP	-55	+125	°C

Saratoga Semiconductor

SSM6170

16K 4,096 Words by 4 Bits BiCMOS TTL Static RAM
with Output Enable

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard Packages**
  24-Pin DIP
  24-Pin SOJ
  24-Pin SOG
- **Output Enable**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

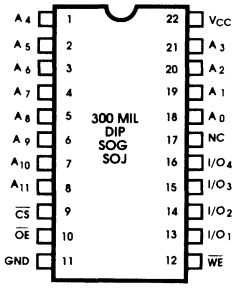
The SSM6170 is a high performance 16K BiCMOS static RAM organized 4096 words by 4 bits. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power consumption (90mA) and high output drive (16mA) of the SSM6170 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are low. Data on the Input/Output pins (I/O_1- I/O_4) is written into the memory cell specified by the 12 bit address placed on the Address Inputs (A_0- A_{11}). With $\overline{CS}$ low, $\overline{WE}$ high and the Output Enable input transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

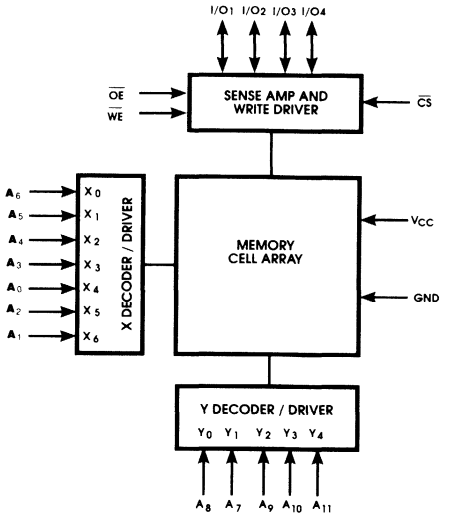
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{11}	Address Inputs
I/O_1 - I/O_4	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply Pins
GND	Ground Pin
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/On	POWER
Read	L	H	L	DO	ACTIVE
Write '0'	L	L	X	L	ACTIVE
Write '1'	L	L	X	H	ACTIVE
Output Disabled	L	H	H	HIGH Z	ACTIVE
Disabled	H	X	X	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM6170 MIN	SSM6170 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC} = max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS} [1]	Output Short Circuit Current	V_{CC} = max; V_{OUT} = GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		90	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

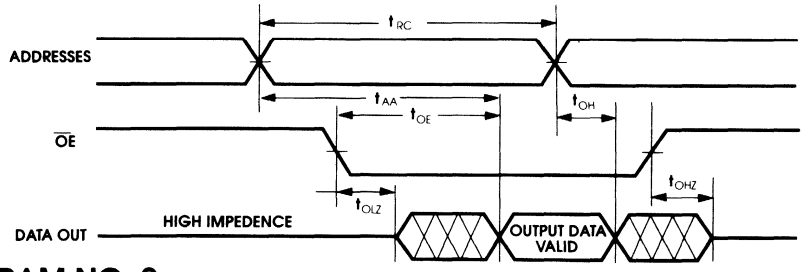
READ CYCLE

PARAMETER	SYMBOL	VALUE				UNIT
		COM SSM6170-20	COM/MIL SSM6170-25	COM/MIL SSM6170-35	MIL SSM6170-45	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
Read Cycle Time	t_{RC}	20	25	35	45	ns
Address Access Time	t_{AA}	20	25	35	45	ns
Chip Select Access Time	t_{ACS}	15	20	25	30	ns
Output Hold from Address Change	t_{OH}	3	3	3	3	ns
Chip Selection to Output in Low Z	t_{LZ} [5]	3	3	3	3	ns
Chip Selection to Output in High Z	t_{HZ} [5]	15	20	25	30	ns
Output Enable to Output Valid	t_{OE}	15	18	20	25	ns
Output Enable to Output in Low Z	t_{OLZ}	0	0	0	0	ns
Output Disable to Output in High Z	t_{OHZ}	12	15	20	25	ns
Chip Selection to Power Up Time	t_{PU} [2]	0	0	0	0	ns
Chip Deselection to Power Down Time	t_{PD} [2]	15	20	25	30	ns

[2] These parameters are sampled and not 100% tested.

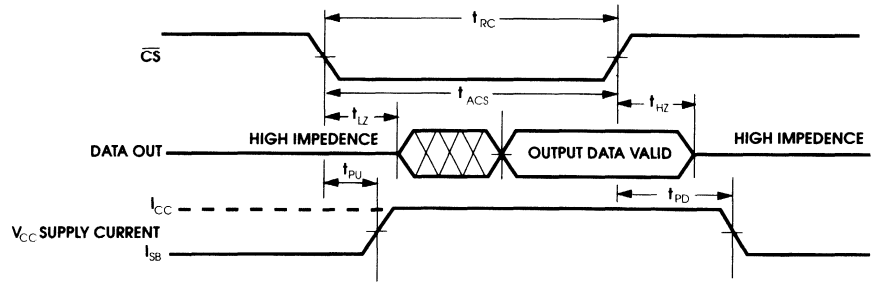
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}. Transition is measured ±500mV from steady state.



READ CYCLE TIMING DIAGRAM NO. 2

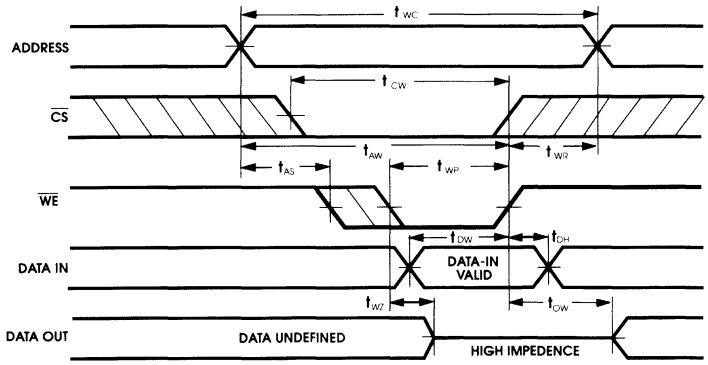
$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state.
Address valid prior to $\overline{CS}$ transition low.



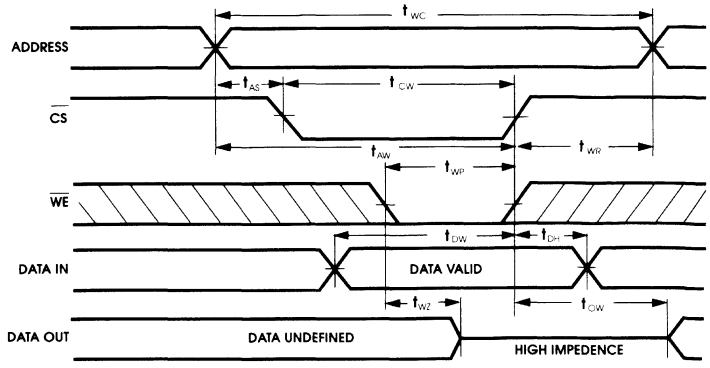
WRITE CYCLE

		VALUE				
		COM SSM6170-20	COM/MIL SSM6170-25	COM/MIL SSM6170-35	MIL SSM6170-45	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	20	25	35	45	ns
Chip Selection to End of Write	t_{CW}	20	25	35	45	ns
Address Valid to End of Write	t_{AW}	20	25	35	45	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	20	25	35	45	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	12	15	20	25	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	10	15	20	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]



WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

CAPACITANCE

PARAMETER	SYMBOL	TYP VALUE	UNIT
Input Pin Capacitance	C_{IN}	5	pF
Output Pin Capacitance	C_{OUT}	7	pF

AC TEST CONDITIONS

[4] Including scope and jig

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Level	1.5V
Output Load	Figures 1 and 2

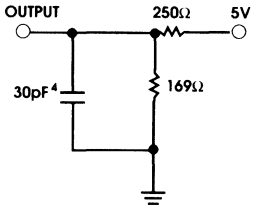


Figure 1

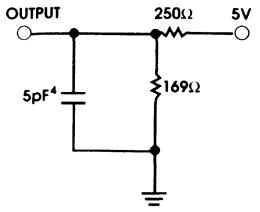
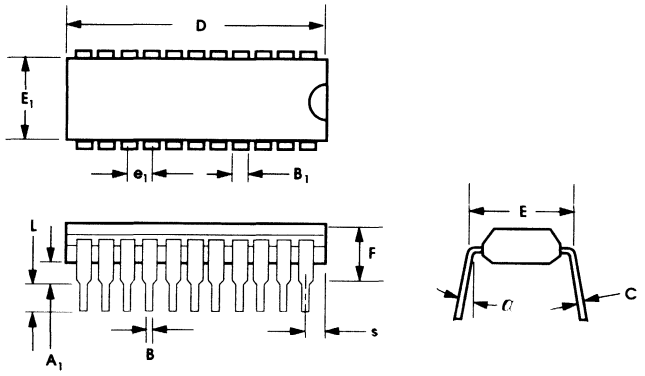


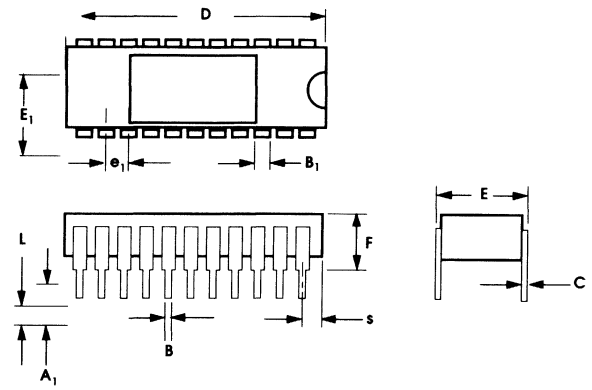
Figure 2

PACKAGE DIMENSIONS



22 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

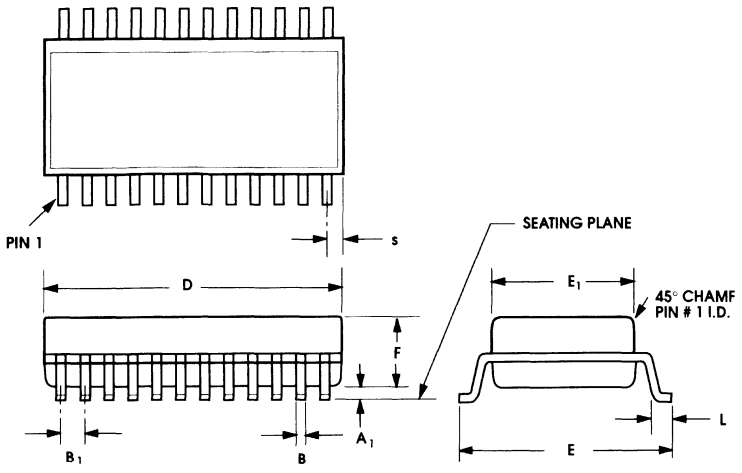
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.055
C	.008	.012
D	1.145	1.155
E	.280	.300
E_1	.250	.270
e_1	.090	.110
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



22 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

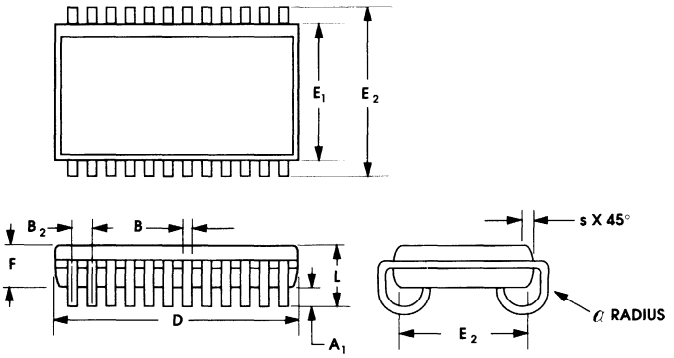
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.085	1.115
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100

PACKAGE DIMENSIONS (CONTINUED)



24 LEAD MOLDED SOG

	INCHES	
PARAMETER	MIN	MAX
A_1	.006	.010
B	.014	.019
B_1	.045	.055
D	.602	.612
E	.400	.416
E_1	.292	.299
F	.090	.094
L	.030	.040
s	.026	.032



24 LEAD MOLDED SOJ

	INCHES	
PARAMETER	MIN	MAX
A_1	.028	.036
B	.014	.019
B_1	.045	.055
D	.602	.612
E	.335	.347
E_1	.292	.299
E_2	.262	.272
F	.090	.094
L	.120	.140
s	.010	.016
α	.031	.042

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM6170-20PC	20ns	22-Pin Plastic DIP	0	+70	°C
SSM6170-25PC	25ns				
SSM6170-35PC	35ns				
SSM6170-20DC	20ns	22-Pin Plastic SOG			
SSM6170-25DC	25ns				
SSM6170-35DC	35ns				
SSM6170-20EC	20ns	22-Pin Plastic SOJ			
SSM6170-25EC	25ns				
SSM6170-35EC	35ns				
SSM6170-20SC	20ns	22-Pin Sidebraze DIP			
SSM6170-25SC	25ns				
SSM6170-35SC	35ns				
SSM6170-25SM	25ns	22-Pin Sidebraze DIP	-55	+125	°C
SSM6170-35SM	35ns				
SSM6170-45SM	45ns				

Saratoga Semiconductor

SSM6171/2

16K 4,096 Words by 4 Bits BiCMOS TTL Static RAM
with Separate Data Inputs and Outputs

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Separate Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard Packages**
  24-Pin DIP
  24-Pin SOJ
  24-Pin SOG
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

The SSM6171/2 is a high performance 16K BiCMOS static RAM organized 4096 words by 4 bits. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power consumption (90mA) and high output drive (16mA) of the SSM6171/2 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

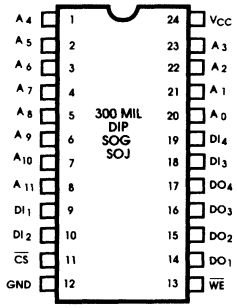
Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are low.

Data on the 4 Input pins (DI_1 - DI_4) are written into the memory cell specified by the 12 bit address placed the Address Inputs (A_0- A_{11}). With $\overline{CS}$ low, $\overline{WE}$ high the of the addressed memory cell is transferred to the 4 Data Output pins (DO_1 - DO_4).

The SSM6171/26 offers a transparent write feature where the Data Output pins (DO_1 - DO_4) remain in a HIGH impedance state when $\overline{CS}$ is HIGH. The SSM6171/2 Data Output pins remain in HIGH impedance state when either $\overline{WE}$ is LOW or $\overline{CS}$ is HIGH.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

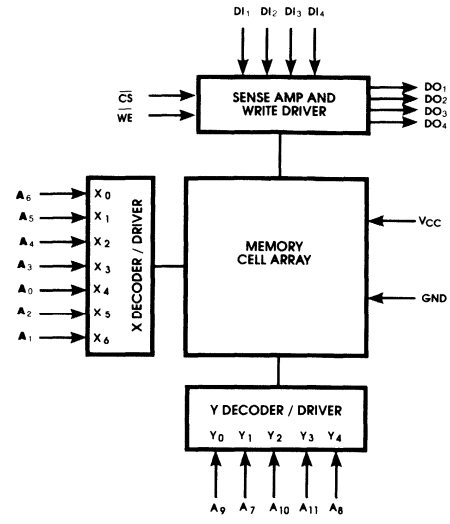
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{11}	Address Inputs
DI_1 - DI_4	Data Inputs
DO_1 - DO_4	Data Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
V_{CC}	Power Supply Pins
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	DIn	DOn		POWER
				SSM6171	SSM6172	
Read	L	H	L	DO	DO	ACTIVE
Write '0'	L	L	L	L	HIGH Z	ACTIVE
Write '1'	L	L	H	H	HIGH Z	ACTIVE
Disabled	H	X	X	HIGH Z	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE		UNIT
		MIN	MAX	
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (V_{CC} = 5V ±10% over specified temperature range)

SYMBOL	PARAMETER	TEST CONDITIONS	SSM6171/2		UNIT
			MIN	MAX	
V_{OH}	Output High Voltage	I_{OH} =-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		90	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

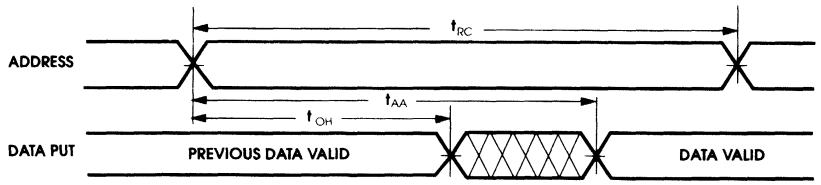
READ CYCLE

PARAMETER	SYMBOL	VALUE								UNIT
		COM SSM6171/2-20		COM/MIL SSM6171/2-25		COM/MIL SSM6171/2-35		MIL SSM6171/2-45		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	20		25		35		45		ns
Address Access Time	t_{AA}		20		25		35		45	ns
Chip Select Access Time	t_{ACS}		15		20		25		30	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Output in LOW Z	t_{LZ}	3		3		3		3		ns
Chip Selection to Output in HIGH Z	t_{HZ}		15		20		25		30	ns
Chip Selection to Power Up Time	t_{PU}[2]	0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}[2]		15		20		25		30	ns

[2] These parameters are sampled and not 100% tested.

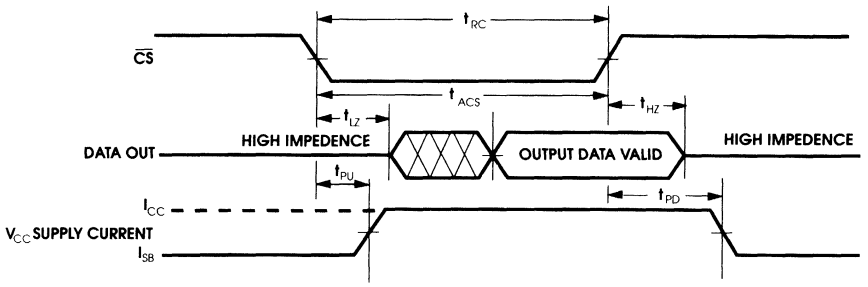
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ is high for Read Cycle. $\overline{CS}$ is low, device is continuously selected. All read Cycle timings are referenced from the last valid address to the first transitioning address.



READ CYCLE TIMING DIAGRAM NO. 2

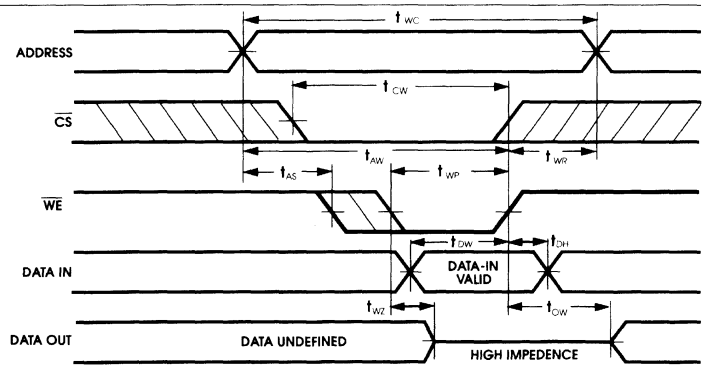
$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.



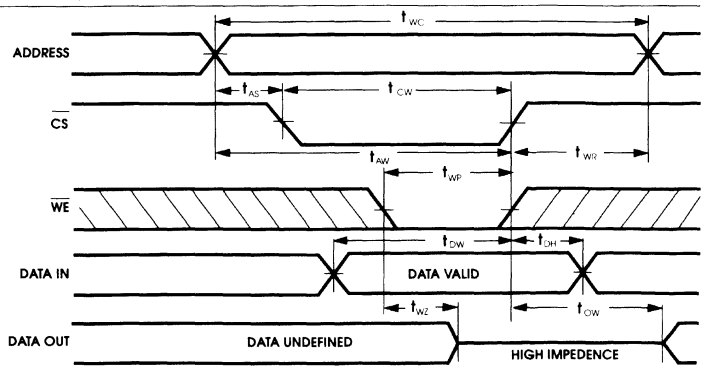
WRITE CYCLE

		VALUE				
		COM SSM6168-20	COM/MIL SSM6168-25	COM/MIL SSM6168-35	MIL SSM6168-45	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	20	25	35	45	ns
Chip Selection to End of Write	t_{CW}	20	25	35	45	ns
Address Valid to End of Write	t_{AW}	20	25	35	45	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	20	25	35	45	ns
Write Recovery Time	t_{WR}	2	0	0	0	ns
Data Valid to End of Write	t_{DW}	12	15	20	25	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Data Valid to Output Valid	t_{IY}[2]	20	20	30	30	ns
Write Enable to Output Valid	t_{WY}[2]	20	20	30	30	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	10	15	20	
Output Active from End of Write	t_{OW}[2]	0	0	0	0	

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED) [3]



WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED) [3]



[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

CAPACITANCE

PARAMETER	SYMBOL	TYP VALUE	UNIT
Input Pin Capacitance	C_{IN}	5	pF
Output Pin Capacitance	C_{OUT}	7	pF

AC TEST CONDITIONS

[4] Including scope and jig

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Level	1.5V
Output Load	Figures 1 and 2

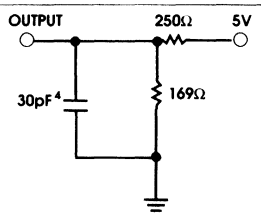


Figure 1

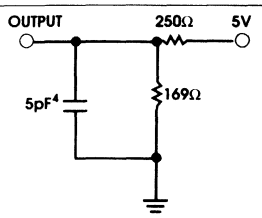
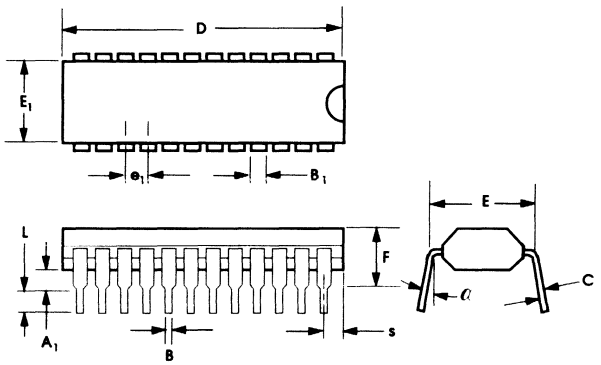


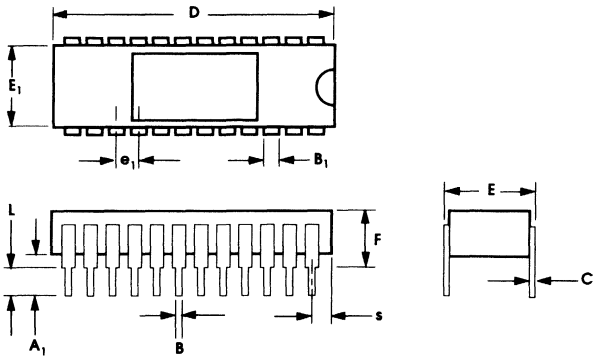
Figure 2

PACKAGE DIMENSIONS



24 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

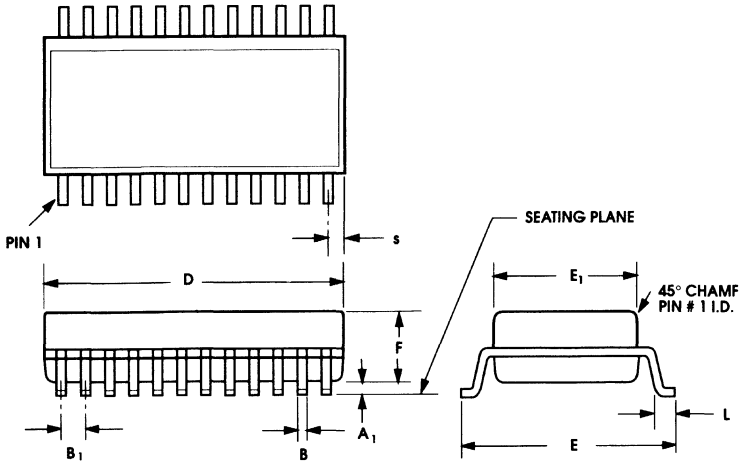
	INCHES	
PARAMETER	MIN	MAX
A_1	.010	
B	.016	.020
B_1	.045	.065
C	.008	.012
D	1.245	1.255
E	.300	.325
E_1	.250	.270
e_1	.095	.105
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



24 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

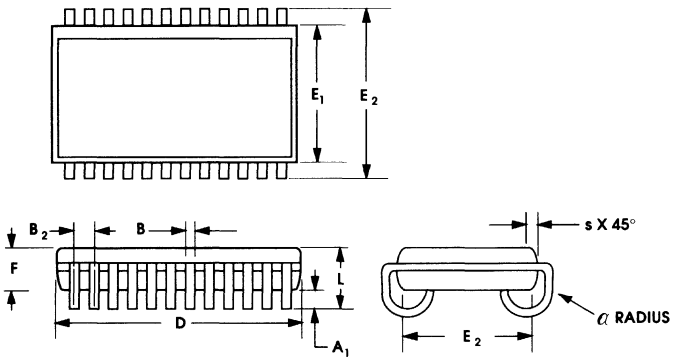
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.185	1.215
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100

PACKAGE DIMENSIONS (CONTINUED)



24 LEAD MOLDED SOG

	INCHES	
PARAMETER	MIN	MAX
A_1	.006	.010
B	.014	.019
B_1	.045	.055
D	.602	.612
E	.400	.416
E_1	.292	.299
F	.090	.094
L	.030	.040
s	.026	.032



24 LEAD MOLDED SOJ

	INCHES	
PARAMETER	MIN	MAX
A_1	.028	.036
B	.014	.019
B_1	.045	.055
D	.602	.612
E	.335	.347
E_1	.292	.299
E_2	.262	.272
F	.090	.094
L	.120	.140
s	.010	.016
α	.031	.042

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM6171/2-20PC	20ns	24-Pin Plastic DIP	0	+70	°C
SSM6171/2-25PC	25ns				
SSM6171/2-35PC	35ns				
SSM6171/2-20DC	20ns	24-Pin Plastic SOG			
SSM6171/2-25DC	25ns				
SSM6171/2-35DC	35ns				
SSM6171/2-20EC	20ns	24-Pin Plastic SOJ			
SSM6171/2-25EC	25ns				
SSM6171/2-35EC	35ns				
SSM6171/2-20SC	20ns	24-Pin Sidebraze DIP			
SSM6171/2-25SC	25ns				
SSM6171/2-35SC	35ns				
SSM6171/2-25SB	25ns	24-Pin Sidebraze DIP	-55	+125	°C
SSM6171/2-35SB	35ns				
SSM6171/2-45SB	45ns				

Saratoga Semiconductor

SSM6116

16K 2,048 Words by 8 Bits BiCMOS TTL Static RAM

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard Packages**
  24-Pin DIP
  24-Pin SOJ
  24-Pin SOG
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

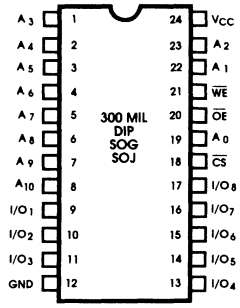
The SSM6116 is a high performance 16K BiCMOS static RAM organized 2048 words by 8 bits. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power consumption (120mA) and high output drive (16mA) of the SSM6116 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are low. Data on the Input/Output pins (I/O_1- I/O_8) is written into the memory cell specified by the 11 bit address placed on the Address Inputs (A_0- A_{10}). With $\overline{CS}$ low, $\overline{WE}$ high and the Output Enable input transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

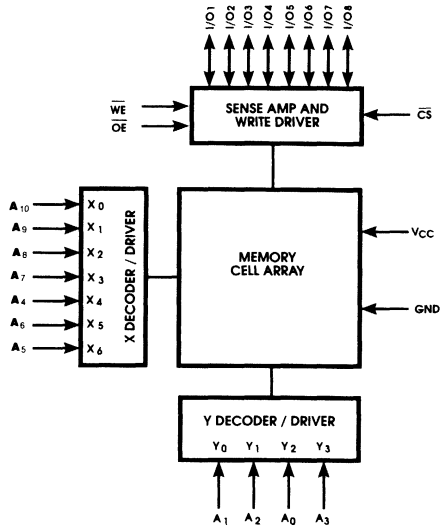
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{10}	Address Inputs
I/O_1 - I/O_8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply Pins
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/On	POWER
Read	L	H	L	DO	ACTIVE
Write '0'	L	L	X	L	ACTIVE
Write '1'	L	L	X	H	ACTIVE
Output Disabled	L	H	H	HIGH Z	ACTIVE
Disabled	H	X	X	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM6118 MIN	SSM6118 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		120	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

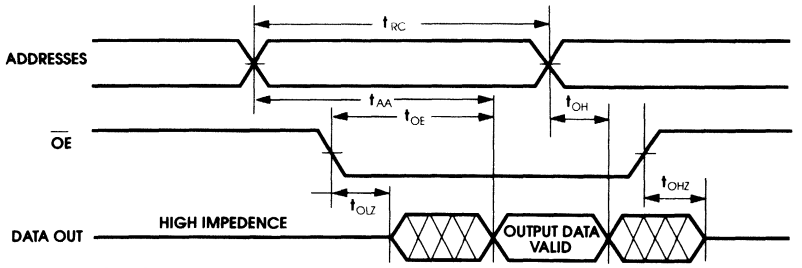
READ CYCLE

PARAMETER	SYMBOL	VALUE COM SSM6116-20 MIN	MAX	COM/MIL SSM6116-25 MIN	MAX	COM/MIL SSM6116-35 MIN	MAX	MIL SSM6116-45 MIN	MAX	UNIT
Read Cycle Time	t_{RC}	20		25		35		45		ns
Address Access Time	t_{AA}		20		25		35		45	ns
Chip Select Access Time	t_{ACS}		15		20		25		30	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Output in LOW Z	t_{LZ} [5]	3		3		3		3		ns
Chip Selection to Output in HIGH Z	t_{HZ} [5]		15		20		25		30	ns
Output Enable to Output Valid	t_{OE}		15		18		20		25	ns
Output Enable to Output in LOW Z	t_{OLZ}	0		0		0		0		ns
Output Disable to Output in HIGH Z	t_{OHZ}		12		15		20		25	ns
Chip Selection to Power Up Time	t_{PU} [2]	0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD} [2]		15		20		25		30	ns

[2] These parameters are sampled and not 100% tested.
[5] These parameters are guaranteed and not tested.

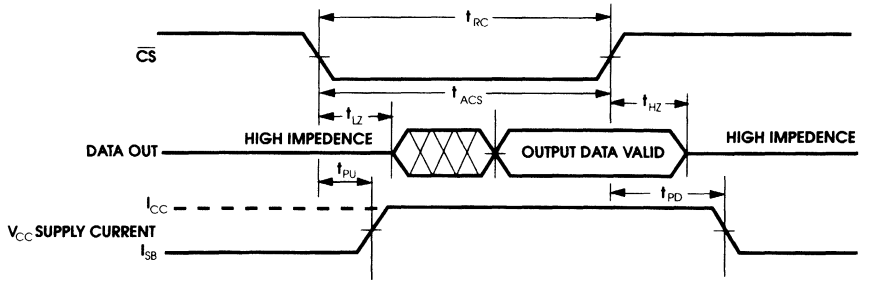
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}. Transition is measured ±500mV from steady state.



READ CYCLE TIMING DIAGRAM NO. 2

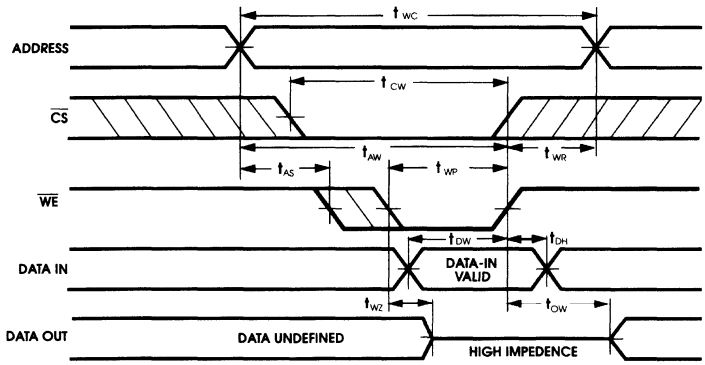
$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state.
Address valid prior to $\overline{CS}$ transition low.



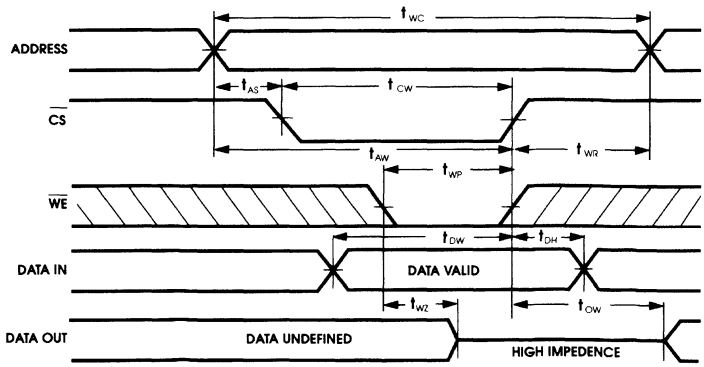
WRITE CYCLE

		VALUE				
		COM/MIL SSM6116-20	COM/MIL SSM6116-25	COM/MIL SSM6116-35	COM/MIL SSM6116-45	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	20	25	35	45	ns
Chip Selection to End of Write	t_{CW}	20	25	35	45	ns
Address Valid to End of Write	t_{AW}	20	25	35	45	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	20	25	35	45	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	12	15	20	25	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	10	15	20	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]



WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

CAPACITANCE

PARAMETER	SYMBOL	TYP VALUE	UNIT
Input Pin Capacitance	C_{IN}	5	pF
Output Pin Capacitance	C_{OUT}	7	pF

AC TEST CONDITIONS

[4] Including scope and jig

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Level	1.5V
Output Load	Figures 1 and 2

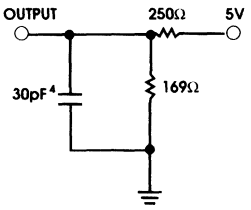


Figure 1

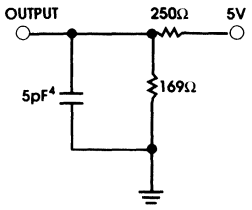
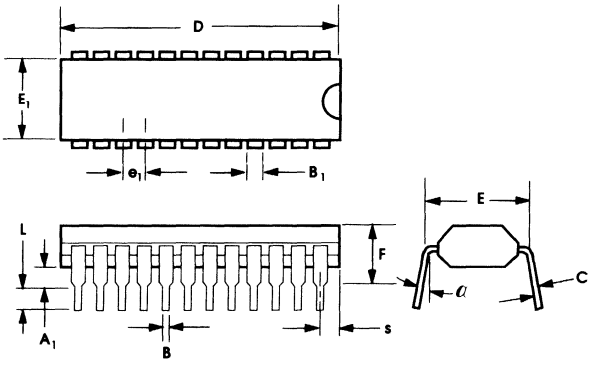


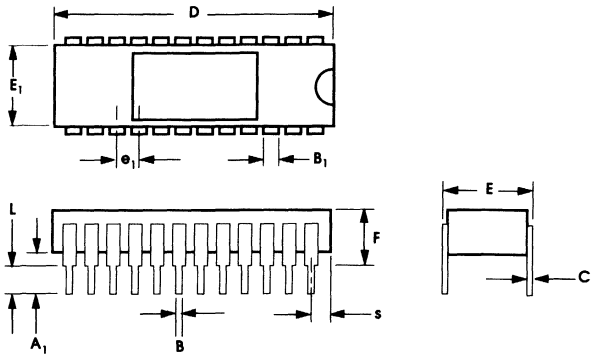
Figure 2

PACKAGE DIMENSIONS



24 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

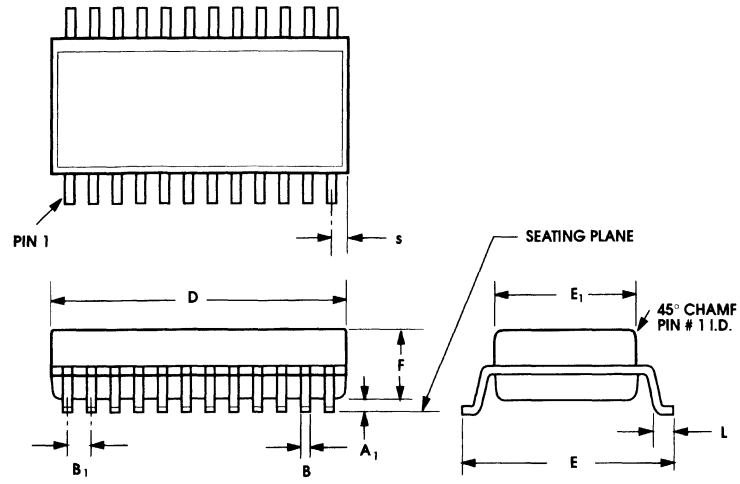
	INCHES	
PARAMETER	MIN	MAX
A_1	.010	
B	.016	.020
B_1	.045	.065
C	.008	.012
D	1.245	1.255
E	.300	.325
E_1	.250	.270
e_1	.095	.105
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



24 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

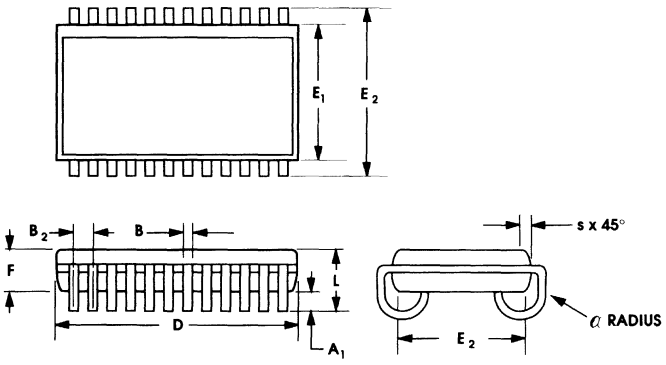
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.185	1.215
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100

PACKAGE DIMENSIONS (CONTINUED)



24 LEAD MOLDED SOG

	INCHES	
PARAMETER	MIN	MAX
A_1	.006	.010
B	.014	.019
B_1	.045	.055
D	.602	.612
E	.400	.416
E_1	.292	.299
F	.090	.094
L	.030	.040
s	.025	.032



24 LEAD MOLDED SOJ

	INCHES	
PARAMETER	MIN	MAX
A_1	.028	.036
B	.014	.019
B_1	.045	.055
D	.602	.612
E	.335	.347
E_1	.292	.299
E_2	.262	.272
F	.090	.094
L	.120	.140
s	.010	.016
α	.031	.042

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM6116-20PC SSM6116-25PC SSM6116-35PC	20ns 25ns 35ns	24-Pin Plastic DIP	0	+70	°C
SSM6116-20DC SSM6116-25DC SSM6116-35DC	20ns 25ns 35ns	24-Pin Plastic SOG			
SSM6116-20EC SSM6116-25EC SSM6116-35EC	20ns 25ns 35ns	24-Pin Plastic SOJ			
SSM6116-20SC SSM6116-25SC SSM6116-35SC	20ns 25ns 35ns	24-Pin Sidebraze DIP			
SSM6116-25SB SSM6116-35SB SSM6116-45SB	25ns 35ns 45ns	24-Pin Sidebraze DIP	-55	+125	°C

Saratoga Semiconductor

SSM7161/2

64K 16,384 Words by 4 Bits BiCMOS TTL Static RAM
with Separate Data Inputs and Outputs

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Separate Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard 28-Pin DIP Packages**
- **Transparent Write (SSM7161)**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

The SSM7161 and SSM7162 are high performance 64K BiCMOS static RAMs organized 16,384 words by 4 bits with separate data inputs and outputs. The devices are targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. They are also designed for use in communication, industrial and military equipment applications.

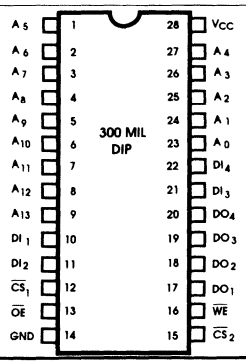
The high speed (20ns), low active power consumption (125mA) and high output drive (16mA) of the SSM7161 and SSM7162 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select inputs ($\overline{CS}_1$, $\overline{CS}_2$) and the Write Enable ($\overline{WE}$) input are low. Data on the four Data Input pins (DI_1 - DI_4) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0 - A_{13}). With $\overline{CS}$ and CS low, $\overline{WE}$ high and the Output Enable input ($\overline{OE}$) low, the content of the addressed memory cell is transfered to the Input/Output pins (DO_1 - DO_4).

The SSM7161 offers a transparent write feature where the Data Output pins (DO_1 - DO_4) contain the information found on the Data Input pins (DI_1 - DI_4) while the device is in write mode. The SSM7162 Data Output pins remain in a high impedance state while the device is in write mode.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

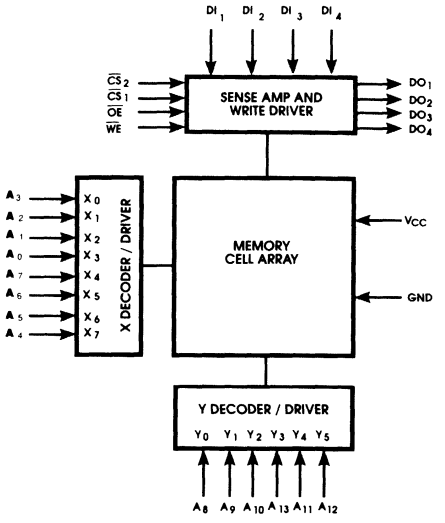
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{13}	Address Inputs
DI_1 - DI_4	Data Inputs
DO_1 - DO_4	Data Outputs
$\overline{CS}_1$, CS_2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power Supply Pin
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	DIn	DOn SSM7161	DOn SSM7162	POWER
Read	L	L	H	L	X	DO	DO	ACTIVE
Write '0'	L	L	L	X	L	L	HIGH Z	ACTIVE
Write '1'	L	L	L	X	H	H	HIGH Z	ACTIVE
Output Disabled	L	L	H	H	X	HIGH Z	HIGH Z	ACTIVE
Disabled	H	X	X	X	X	HIGH Z	HIGH Z	STANDBY
Disabled	X	H	X	X	X	HIGH Z	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM7161/2 MIN	SSM7161/2 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		125	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

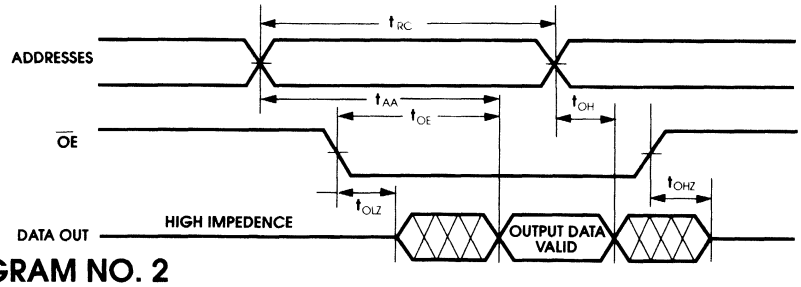
READ CYCLE

PARAMETER	SYMBOL	VALUE				UNIT
		COM SSM7161/2-20	COM/MIL SSM7161/2-25	COM/MIL SSM7161/2-35	MIL SSM7161/2-45	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
Read Cycle Time	t_{RC}	20	25	35	45	ns
Address Access Time	t_{AA}	20	25	35	45	ns
Chip Select Access Time	t_{ACS}	15	20	25	30	ns
Output Hold from Address Change	t_{OH}	3	3	3	3	ns
Chip Selection to Output in LOW Z	t_{LZ}	3	3	3	3	ns
Chip Selection to Output in HIGH Z	t_{HZ}	15	20	25	30	ns
Output Enable to Output Valid	t_{OE}	15	18	20	25	ns
Output Enable to Output in LOW Z	t_{OLZ}	0	0	0	0	ns
Output Disable to Output in HIGH Z	t_{OHZ}	12	15	20	25	ns
Chip Selection to Power Up Time	t_{PU}[2]	0	0	0	0	ns
Chip Deselection to Power Down Time	t_{PD}[2]	15	20	25	30	ns

[2] These parameters are sampled and not 100% tested.

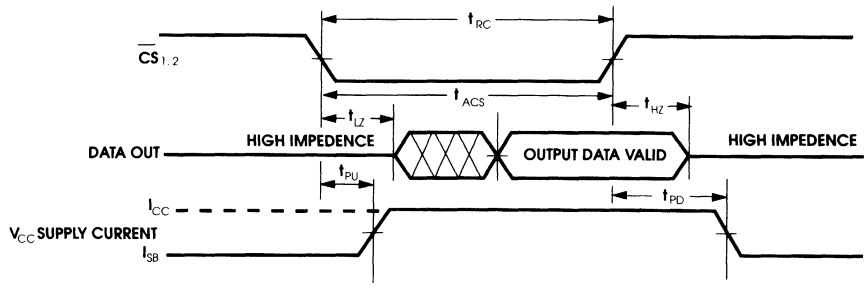
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ = V_{IH}, $\overline{CS}_{1,2}$ = V_{IL}. Transition is measured ±500mV from steady state.



READ CYCLE TIMING DIAGRAM NO. 2

$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state.
Address valid prior to $\overline{CS}$ transition low.



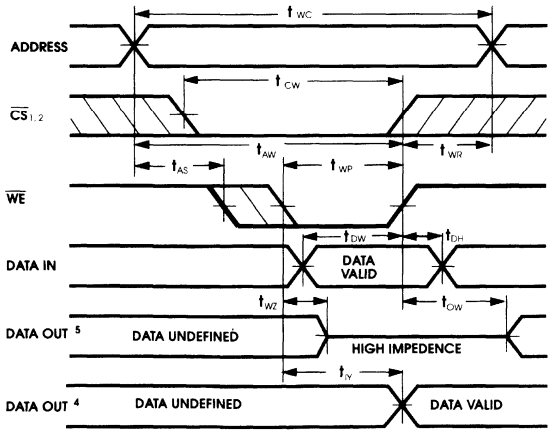
WRITE CYCLE

		VALUE				
		COM SSM7161/2-20	COM/MIL SSM7161/2-25	COM/MIL SSM7161/2-35	MIL SSM7161/2-45	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	20	25	35	45	ns
Chip Selection to End of Write	t_{CW}	20	25	35	45	ns
Address Valid to End of Write	t_{AW}	20	25	35	45	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	20	25	35	45	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	12	15	20	25	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Data Valid to Output Valid	t_{IY}[2]	20	20	30	35	ns
Write Enable to Output Valid	t_{WY}[2]	20	20	30	35	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	10	15	20	ns
Output Active from End of Write	t_{OW}[2]	0	0	3	3	ns

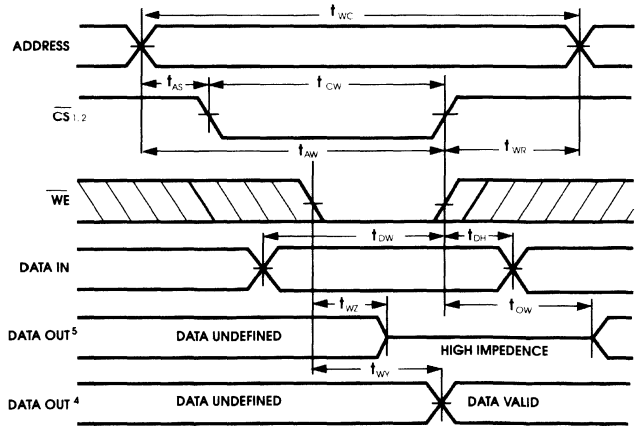
[1] These parameters are sampled and not 100% tested.

WRITE CYCLE TIMING DIAGRAMS

(WE CONTROLLED) [3]

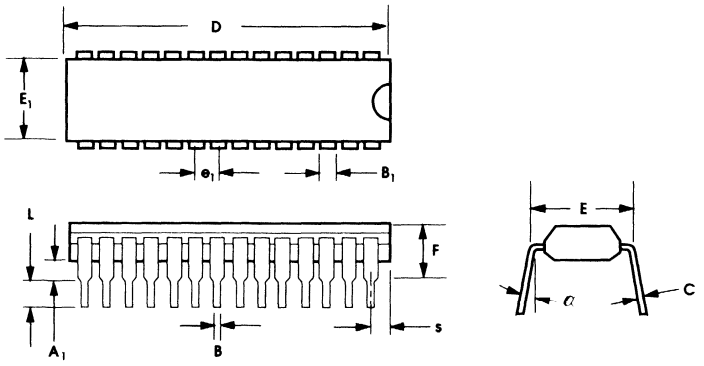


NO.2 ($CS_{1,2}$ CONTROLLED) [3]



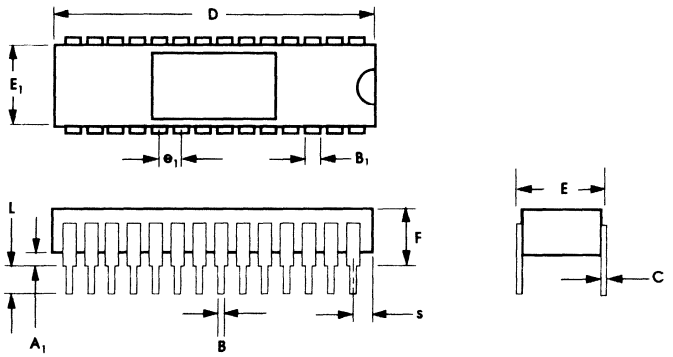
[3] If CS goes high simultaneously with WE high, the output remains in a high impedence state. CS or WE must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

PACKAGE DIMENSIONS



28 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.065
C	.008	.012
D	1.345	1.355
E	.300	.325
E_1	.270	.290
e_1	.090	.110
F		.170
L	.125	.135
s	.020	.030
α	0°	15°



28 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.385	1.415
E	.285	.305
E_1	.290	.310
e_1	.090	.110
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

PART NUMBER	SPEED	TEMPERATURE RANGE MIN	MAX	UNIT
SSM7161-20PC	20ns	0	+70	°C
SSM7161-25PC	25ns			
SSM7161-35PC	35ns			
SSM7161-20SC	20ns			
SSM7161-25SC	25ns			
SSM7161-35SC	35ns			
SSM7161-25SB	25ns	-55	+125	°C
SSM7161-35SB	35ns			
SSM7161-45SB	45ns			
SSM7162-20PC	20ns	0	+70	°C
SSM7162-25PC	25ns			
SSM7162-35PC	35ns			
SSM7162-20SC	20ns			
SSM7162-25SC	25ns			
SSM7162-35SC	35ns			
SSM7162-25SB	25ns	-55	+125	°C
SSM7162-35SB	35ns			
SSM7162-45SB	45ns			

Saratoga Semiconductor

SSM7166

64K 16,384 Words by 4 Bits BiCMOS TTL Static RAM
with Output Enable

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard 24-Pin Packages**
- **Output Enable**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

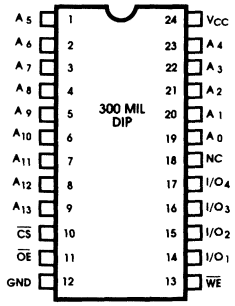
The SSM7166 is a high performance 64K BiCMOS static RAM organized 16,384 words by 4 bits. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power consumption (125mA) and high output drive (16mA) of the SSM7166 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are LOW. Data on the Input/Output pins (I/O_1- I/O_4) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0- A_{13}). With $\overline{CS}$ LOW, $\overline{WE}$ HIGH and the Output Enable input ($\overline{OE}$) LOW, the content of the addressed memory cell is transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

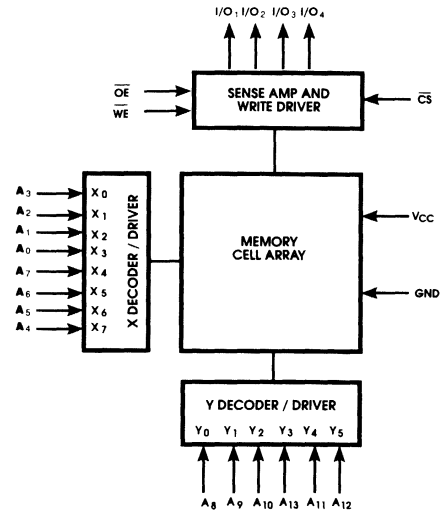
PIN CONFIGURATION



PIN IDENTIFICATION

A_0-A_{13}	Address Inputs
I/O_1-I/O_4	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power Supply Pin
GND	Ground Pin
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/On	POWER
Read	L	H	L	DO	ACTIVE
Write '0'	L	L	X	L	ACTIVE
Write '1'	L	L	X	H	ACTIVE
Output Disabled	L	H	H	HIGH Z	ACTIVE
Disabled	H	X	X	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM7166 MIN	SSM7166 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH} =-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		125	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

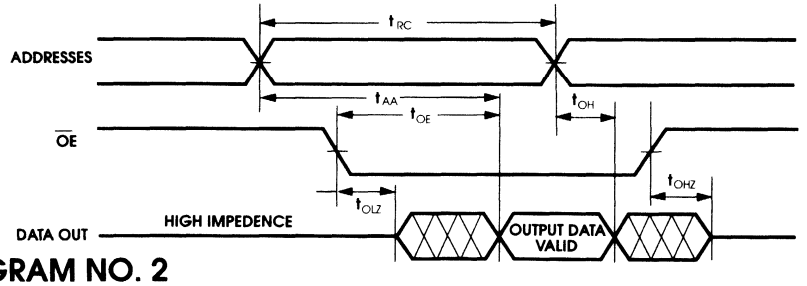
READ CYCLE

PARAMETER	SYMBOL	VALUE								UNIT
		COM SSM7166-20		COM/MIL SSM7166-25		COM/MIL SSM7166-35		MIL SSM7166-45		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	20		25		35		45		ns
Address Access Time	t_{AA}		20		25		35		45	ns
Chip Select Access Time	t_{ACS}		15		20		25		30	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Output in LOW Z	t_{LZ}	3		3		3		3		ns
Chip Selection to Output in HIGH Z	t_{HZ}		15		20		25		30	ns
Output Enable to Output Valid	t_{OE}		15		18		20		25	ns
Output Enable to Output in LOW Z	t_{OLZ}	0		0		0		0		ns
Output Disable to Output in HIGH Z	t_{OHZ}		12		15		20		25	ns
Chip Selection to Power Up Time	t_{PU}[2]	0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}[2]		15		20		25		30	ns

[2] These parameters are sampled and not 100% tested.

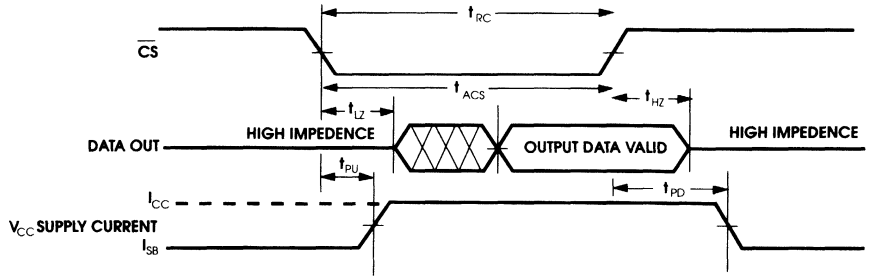
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}. Transition is measured ±500mV from steady state.



READ CYCLE TIMING DIAGRAM NO. 2

$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.

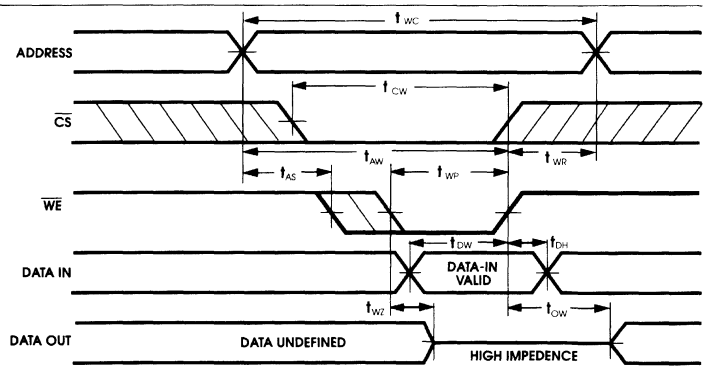


WRITE CYCLE

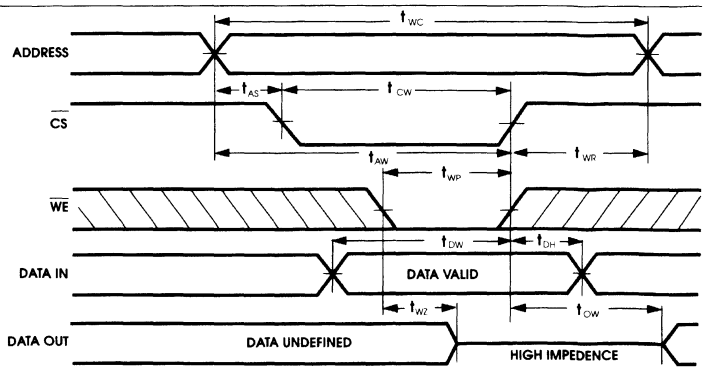
		VALUE				
		COM SSM7166-20	COM/MIL SSM7166-25	COM/MIL SSM7166-35	MIL SSM7166-45	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	20	25	35	45	ns
Chip Selection to End of Write	t_{CW}	20	25	35	45	ns
Address Valid to End of Write	t_{AW}	20	25	35	45	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	20	25	35	45	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	12	15	20	25	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	10	15	20	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

These parameters are sampled and not 100% tested.

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]

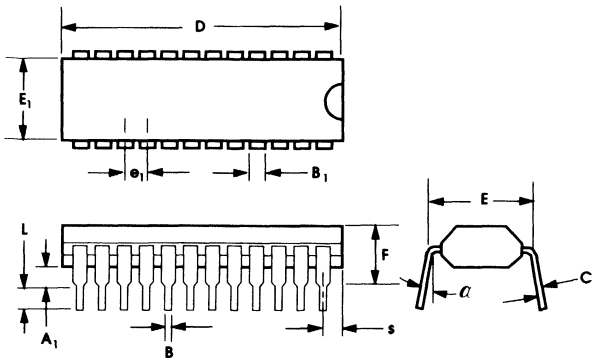


WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



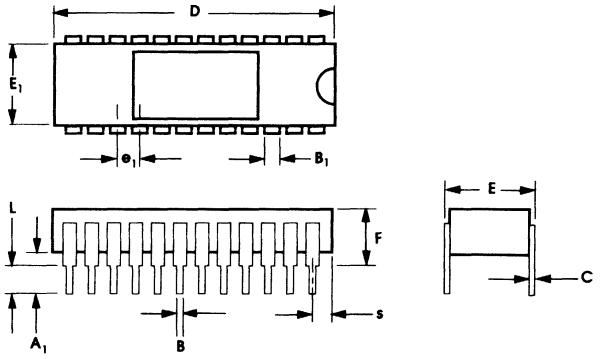
[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

PACKAGE DIMENSIONS



24 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.010	
B	.016	.020
B_1	.045	.065
C	.008	.012
D	1.245	1.255
E	.300	.325
E_1	.250	.270
e_1	.095	.105
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



24 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.185	1.215
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM7166-20PC	20ns	24-Pin Plastic DIP	0	+70	°C
SSM7166-25PC	25ns				
SSM7166-35PC	35ns				
SSM7166-20SC	20ns	24-Pin Sidebraze DIP			
SSM7166-25SC	25ns				
SSM7166-35SC	35ns				
SSM7166-25SB	25ns	24-Pin Sidebraze DIP	-55	+125	°C
SSM7166-35SB	35ns				
SSM7166-45SB	45ns				

Saratoga Semiconductor

SSM7188

64K 16,384 Words by 4 Bits BiCMOS TTL Static RAM

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard 22-Pin Packages**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

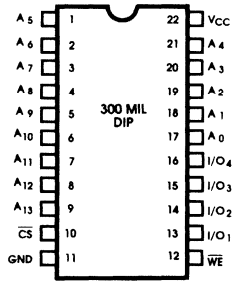
The SSM7188 is a high performance 64K BiCMOS static RAM organized 16,384 words by 4 bits. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power consumption (125mA) and high output drive (16mA) of the SSM7188 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are LOW. Data on the Input/Output pins (I/O_1- I/O_4) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0 A_{13}). With CS LOW and WE HIGH, the content of the addressed memory cell is transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

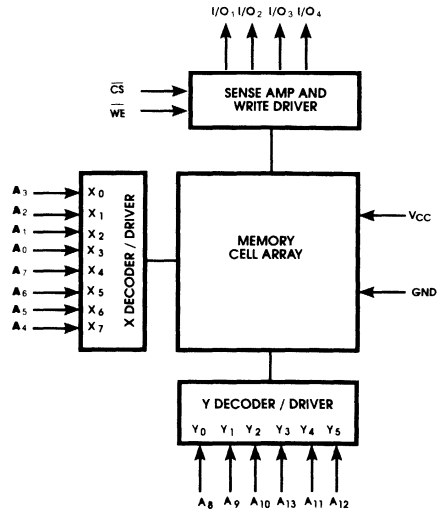
PIN CONFIGURATION



PIN IDENTIFICATION

A_0-A_{13}	Address Inputs
I/O_1-I/O_4	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power Supply Pin
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	I/On	POWER
Read	L	H	DO	ACTIVE
Write '0'	L	L	L	ACTIVE
Write '1'	L	L	H	ACTIVE
Disabled	H	X	HIGH Z	STANDBY

H = High Voltage Level
L = Low Voltage Level
X = Irrelevant
DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM7188 MIN	SSM7188 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		125	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

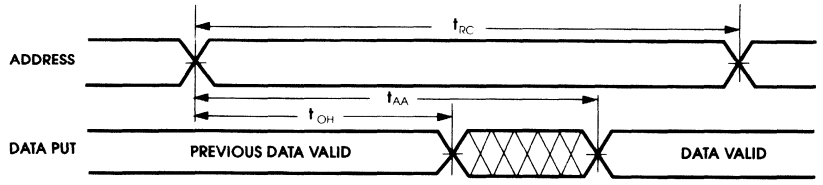
READ CYCLE

PARAMETER	SYMBOL	VALUE								UNIT
		COM SSM7188-20		COM/MIL SSM7188-25		COM/MIL SSM7188-35		MIL SSM7188-45		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	20		25		35		45		ns
Address Access Time	t_{AA}		20		25		35		45	ns
Chip Select Access Time	t_{ACS}		15		20		25		30	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Output in LOW Z	t_{LZ}	3		3		3		3		ns
Chip Selection to Output in HIGH Z	t_{HZ}		15		20		25		30	ns
Chip Selection to Power Up Time	t_{PU}[2]	0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}[2]		15		20		25		30	ns

[2] These parameters are sampled and not 100% tested.

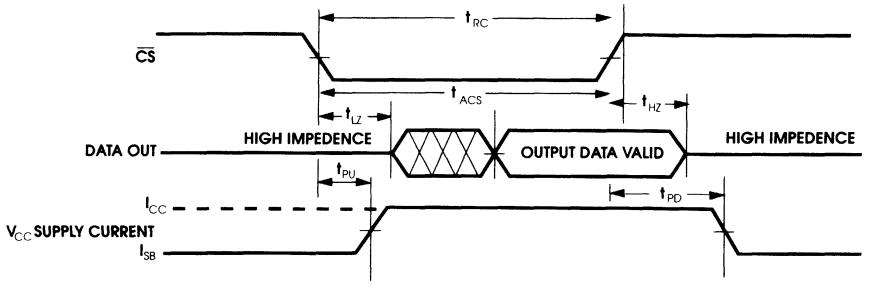
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ is high for Read Cycle. $\overline{CS}$ is low, device is continuously selected. All read Cycle timings are referenced from the last valid address to the first transitioning address.



READ CYCLE TIMING DIAGRAM NO. 2

$\overline{WE}$ = V_{IH} , $\overline{OE}$ = V_{IL} . Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.

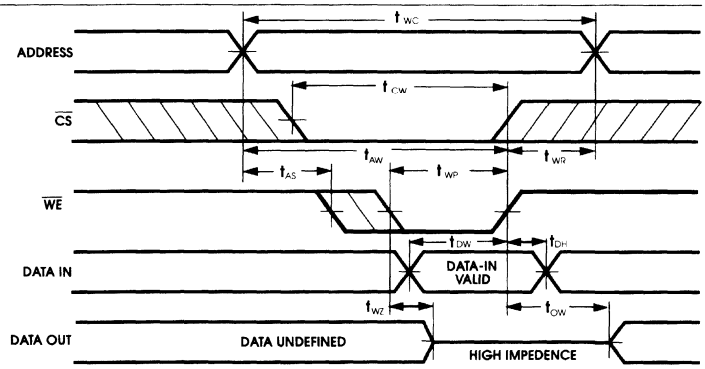


WRITE CYCLE

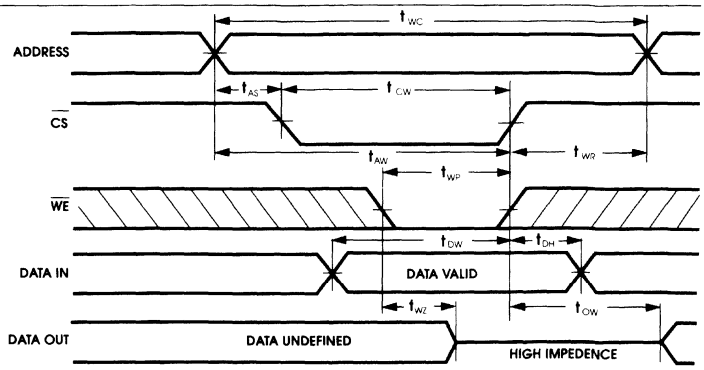
		VALUE				
		COM SSM7188-20	COM/MIL SSM7188-25	COM/MIL SSM7188-35	MIL SSM7188-45	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	20	25	35	45	ns
Chip Selection to End of Write	t_{CW}	20	25	35	45	ns
Address Valid to End of Write	t_{AW}	20	25	35	45	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	20	25	35	45	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	12	15	20	25	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	10	15	20	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

[2] These parameters are sampled and not 100% tested.

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED)[3]

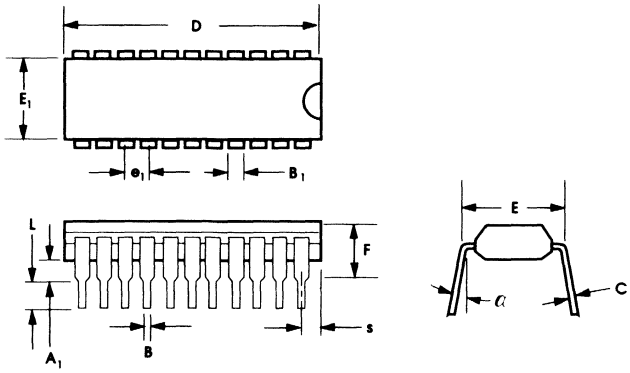


WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED)[3]



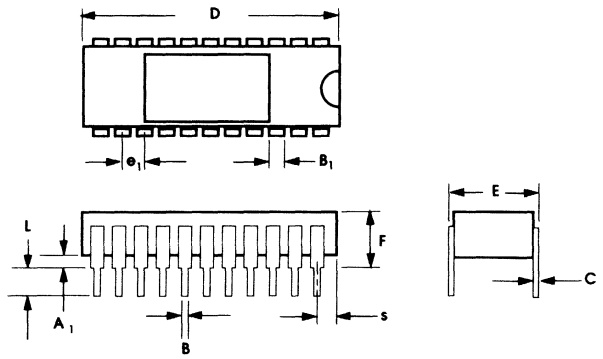
[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

PACKAGE DIMENSIONS



22 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.055
C	.008	.012
D	1.145	1.155
E	.280	.300
E_1	.250	.270
e_1	.090	.110
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



22 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.085	1.115
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM7188-20PC	20ns	22-Pin Plastic DIP	0	+70	°C
SSM7188-25PC	25ns				
SSM7188-35PC	35ns				
SSM7188-20SC	20ns	22-Pin Sidebraze DIP			
SSM7188-25SC	25ns				
SSM7188-35SC	35ns				
SSM7188-25SB	25ns	22-Pin Sidebraze DIP	-55	+125	°C
SSM7188-35SB	35ns				
SSM7188-45SB	45ns				

Saratoga Semiconductor

SSM7198

64K 16,384 Words by 4 Bits BiCMOS TTL Static RAM
with Output Enable and Dual Chip Select Inputs

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard 24-Pin DIP Packages**
- **Output enable & Dual Chip Select**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

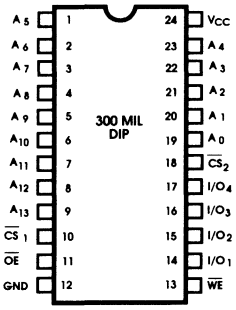
The SSM7198 is a high performance 64K BiCMOS static RAM organized 16,384 words by 4 bits. The device is targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. It is also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power consumption (125mA) and high output drive (16mA) of the SSM7198 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select (CS) and Write Enable ($\overline{WE}$) inputs are low. Data on the Input/Output pins (I/O_1- I/O_4) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0- A_{13}). With $\overline{CS}_1$ and $\overline{CS}_2$ low, $\overline{WE}$ high and the Output Enable input ($\overline{OE}$) low, the content of the addressed memory cell is transferred to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

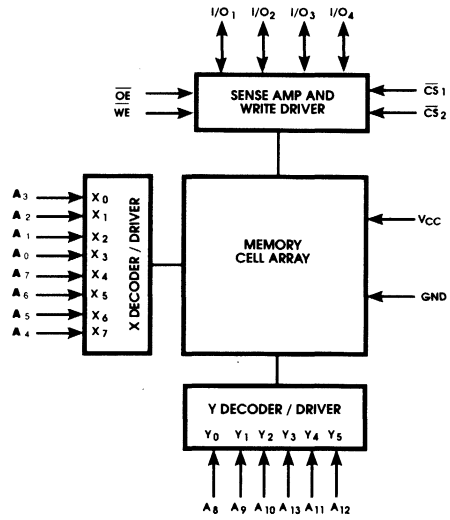
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{13}	Address Inputs
I/O_1 - I/O_4	Data Inputs/Outputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply Pins
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	I/On	POWER
Read	L	L	H	L	DO	ACTIVE
Write '0'	L	L	L	X	L	ACTIVE
Write '1'	L	L	L	X	H	ACTIVE
Output Disabled	L	L	H	H	HIGH Z	ACTIVE
Disabled	H	X	X	X	HIGH Z	STANDBY
Disabled	X	H	X	X	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM7198 MIN	SSM7198 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		125	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

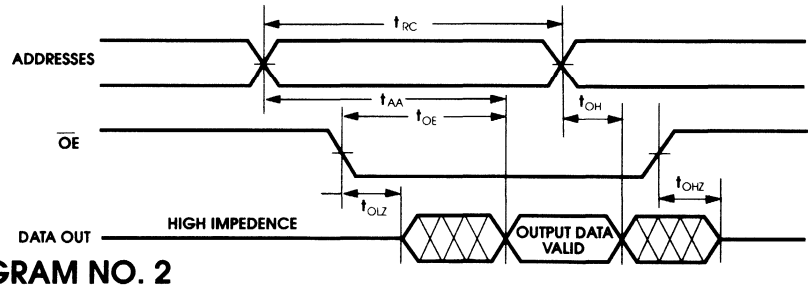
READ CYCLE

PARAMETER	SYMBOL	VALUE				UNIT
		COM SSM7198-20	COM/MIL SSM7198-25	COM/MIL SSM7198-35	MIL SSM7198-45	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
Read Cycle Time	t_{RC}	20	25	35	45	ns
Address Access Time	t_{AA}	20	25	35	45	ns
Chip Select Access Time	t_{ACS}	15	20	25	30	ns
Output Hold from Address Change	t_{OH}	3	3	3	3	ns
Chip Selection to Output in LOW Z	t_{LZ}	3	3	3	3	ns
Chip Selection to Output in HIGH Z	t_{HZ}	15	20	25	30	ns
Output Enable to Output Valid	t_{OE}	15	18	20	25	ns
Output Enable to Output in LOW Z	t_{OLZ}	0	0	0	0	ns
Output Disable to Output in HIGH Z	t_{OHZ}	12	15	20	25	ns
Chip Selection to Power Up Time	t_{PU}[2]	0	0	0	0	ns
Chip Deselection to Power Down Time	t_{PD}[2]	15	20	25	30	ns

[2] These parameters are sampled and not 100% tested.

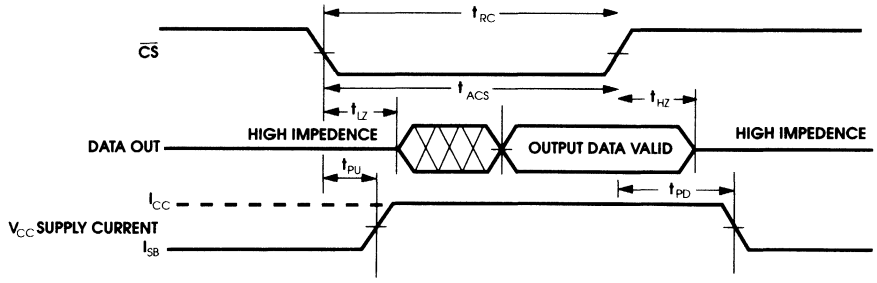
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ = V_{IH}, $\overline{CS}_{1,2}$ = V_{IL}. Transition is measured ±500mV from steady state.



READ CYCLE TIMING DIAGRAM NO. 2

$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state. Address valid prior to $\overline{CS}$ transition low.

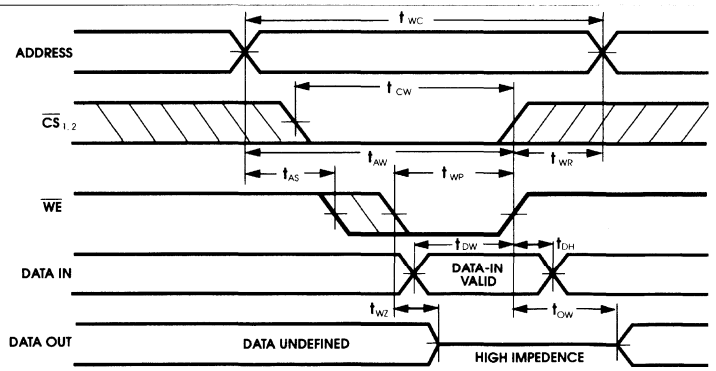


WRITE CYCLE

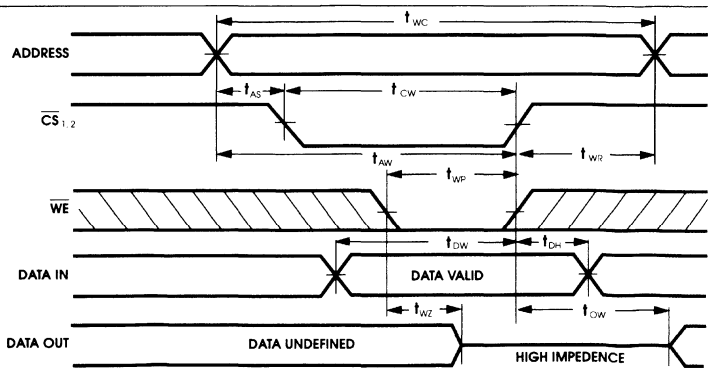
		VALUE								
		COM SSM7198-20		COM/MIL SSM7198-25		COM/MIL SSM7198-35		MIL SSM7198-45		
	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Write Cycle Time	t_{WC}	20		25		35		45		ns
Chip Selection to End of Write	t_{CW}	20		25		35		45		ns
Address Valid to End of Write	t_{AW}	20		25		35		45		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	20		25		35		45		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Data Valid to End of Write	t_{DW}	12		15		20		25		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write Enable to Output in HIGH Z	t_{WZ} [2]		8		10		15		20	ns
Output Active from End of Write	t_{OW} [2]	0		0		0		0		ns

[2] These parameters are sampled and not 100% tested.

WRITE CYCLE TIMING DIAGRAM NO.1 (WE CONTROLLED) [3]

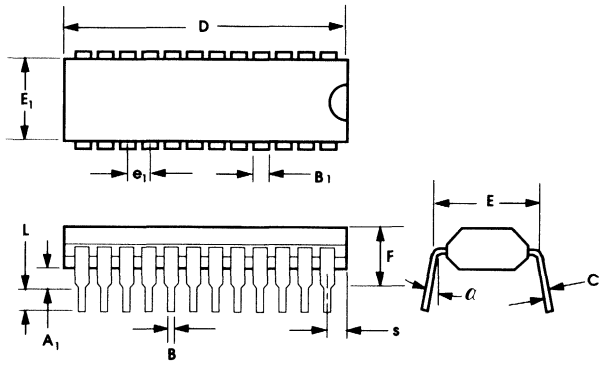


WRITE CYCLE TIMING DIAGRAM NO.2 (CS CONTROLLED) [3]



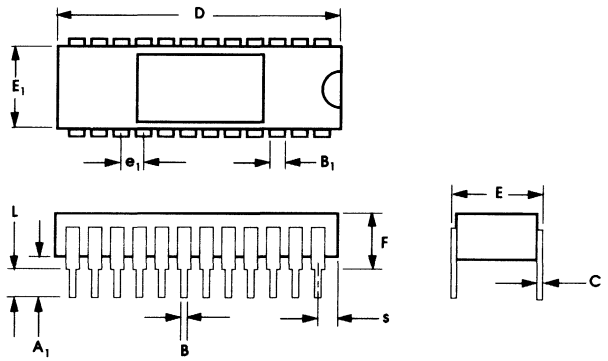
[3] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

PACKAGE DIMENSIONS



24 LEAD 300 MIL PLASTIC IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.010	
B_1	.045	.065
B	.016	.020
C	.008	.012
D	1.245	1.255
E	.300	.325
E_1	.250	.270
e_1	.095	.105
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



24 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.185	1.215
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM7198-20PC	20ns	24-Pin Plastic DIP	0	+70	°C
SSM7198-25PC	25ns				
SSM7198-35PC	35ns				
SSM7198-20SC	20ns	24-Pin Sidebraze DIP			
SSM7198-25SC	25ns				
SSM7198-35SC	35ns				
SSM7198-25SB	25ns	24-Pin Sidebraze DIP	-55	+125	°C
SSM7198-35SB	35ns				
SSM7198-45SB	45ns				

Saratoga Semiconductor

SSM7164

64K 8,192 Words by 8 Bits BiCMOS TTL Static RAM

FEATURES

- **Fast Access Times**
  20/25/35ns Commercial Temperature
  25/35/45ns Military Temperature
- **Common Data Inputs & Outputs**
- **Full Military 883C Level B Compliant**
- **Industry Standard 28-Pin DIP Packages**
- **Output Enable & Dual Chip Select**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

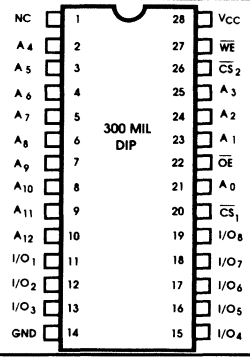
The SSM7164 is a high performance 64K BiCMOS static RAM organized 8,192 words by 8 bits. The devices are targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. They are also designed for use in communication, industrial and military equipment applications.

The high speed (20ns), low active power (825mW) and high output drive (16mA) of the SSM7164 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select One ($\overline{CS}_1$) input is LOW, Chip Select Two ($\overline{CS}_2$) input is HIGH and the Write Enable ($\overline{WE}$) input is LOW. Data on Input/Output pins (I/O_1 - I/O_8) is written into the memory cell specified by the 13 bit address placed on the Address Inputs (A_0- A_{12}). With $\overline{CS}_1$ LOW, $\overline{CS}_2$ HIGH,Output Enable ($\overline{OE}$) LOW, and $\overline{WE}$ high, the content of the addressed memory cell is transfered to the Input/Output pins.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

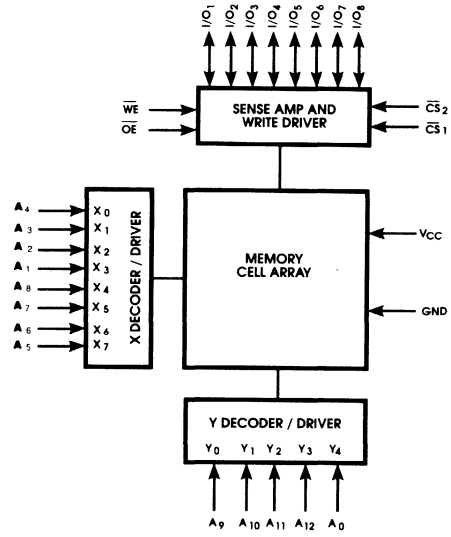
PIN CONFIGURATION



PIN IDENTIFICATION

A_0- A_{12}	Address Inputs
I/O_1 - I/O_8	Data Inputs/Outputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply Pin
GND	Ground Pin
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	I/On	POWER
Read	L	H	H	L	DO	ACTIVE
Write '0'	L	H	L	X	L	ACTIVE
Write '1'	L	H	L	X	H	ACTIVE
Output Disabled	L	H	H	H	HIGH Z	ACTIVE
Disabled	H	X	X	X	HIGH Z	STANDBY
Disabled	X	L	X	X	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operaating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM7164 MIN	SSM7164 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH}=-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=-16mA ; V_{CC} = min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		150	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

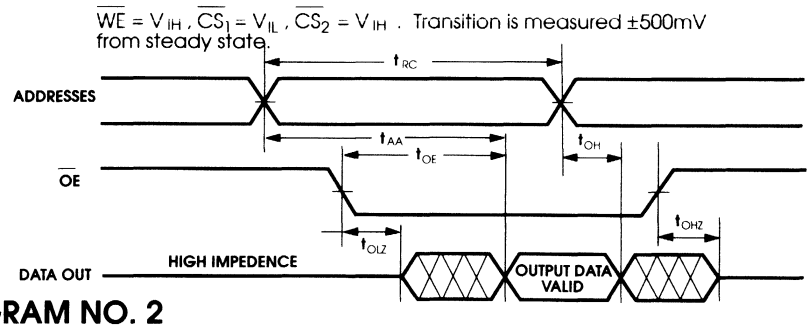
AC CHARACTERISTICS

READ CYCLE

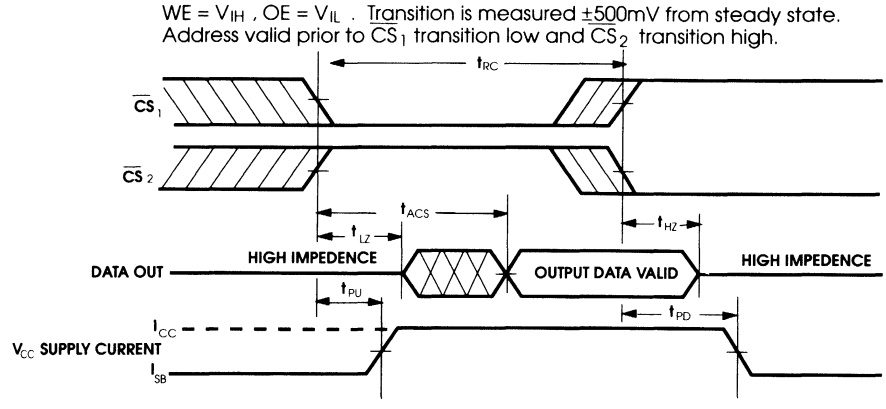
PARAMETER	SYMBOL	VALUE								UNIT
		COM SSM7164-20		COM/MIL SSM7164-25		COM/MIL SSM7164-35		MIL SSM7164-45		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	20		25		35		45		ns
Address Access Time	t_{AA}		20		25		35		45	ns
Chip Select Access Time	t_{ACS}		15		20		25		30	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Output in LOW Z	t_{LZ}	3		3		3		3		ns
Chip Deselection to Output in HIGH Z	t_{HZ}		15		20		25		30	ns
Output Enable to Output Valid	t_{OE}		15		18		20		25	ns
Output Enable to Output in LOW Z	t_{OLZ}	0		0		0		0		ns
Output Disable to Output in HIGH Z	t_{OHZ}		12		15		20		25	ns
Chip Selection to Power Up Time	t_{PU}[2]	0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}[2]		15		20		25		30	ns

[2] These parameters are sampled and not 100% tested.

READ CYCLE TIMING DIAGRAM NO. 1



READ CYCLE TIMING DIAGRAM NO. 2



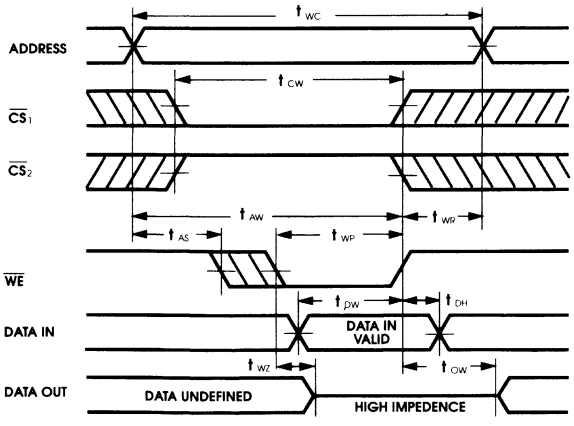
WRITE CYCLE

PARAMETER	SYMBOL	VALUE COM SSM7164-20 MIN	MAX	COM/MIL SSM7164-25 MIN	MAX	COM/MIL SSM7164-35 MIN	MAX	MIL SSM7164-45 MIN	MAX	UNIT
Write Cycle Time	t_{WC}	20		25		35		45		ns
Chip Selection to End of Write	t_{CW}	20		25		35		45		ns
Address Valid to End of Write	t_{AW}	20		25		35		45		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	20		25		35		45		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Data Valid to End of Write	t_{DW}	12		15		25		25		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write Enable to Output in HIGH Z	t_{WZ}[2]		8		10		15		20	ns
Output Active from End of Write	t_{OW}[2]	0		0		0		0		ns

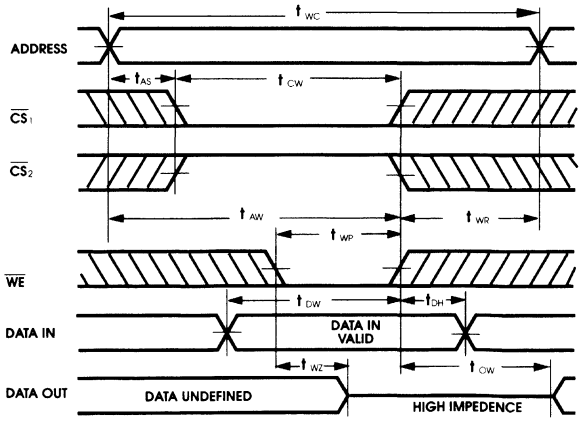
[2] These parameters are sampled and not 100% tested.

WRITE CYCLE TIMING DIAGRAMS

(WE CONTROLLED) [3]

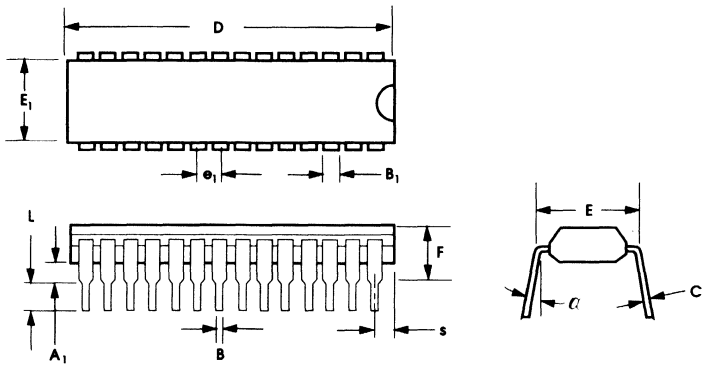


NO.2 ($CS_{1,2}$ CONTROLLED) [3]



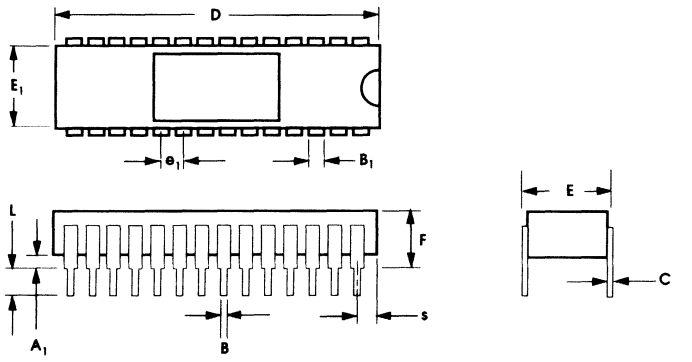
[3] If $\overline{CS}_1$ goes high or $\overline{CS}_2$ goes low simultaneously with $\overline{WE}$ high, the output remains in a high impedence state. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

PACKAGE DIMENSIONS



28 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.055
C	.008	.012
D	1.345	1.355
E	.300	.325
E_1	.270	.290
e_1	.090	.110
F		.170
L	.125	.135
s	.020	.030
α	0°	15°



28 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.385	1.415
E	.285	.305
E_1	.290	.310
e_1	.090	.110
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM7164-20PC	20ns	28-Pin Plastic DIP	0	+70	°C
SSM7164-25PC	25ns				
SSM7164-35PC	35ns				
SSM7164-20SC	20ns	28-Pin Sidebraze DIP			
SSM7164-25SC	25ns				
SSM7164-35SC	35ns				
SSM7164-25SB	25ns	28-Pin Sidebraze DIP	-55	+125	°C
SSM7164-35SB	35ns				
SSM7164-45SB	45ns				

Saratoga Semiconductor

SSM7192/5

16K by 4 Bit BiCMOS TTL Synchronous Static RAM
with Transparent Outputs

PRELIMINARY INFORMATION

FEATURES

- **High Performance**
  20ns Access Time
  8ns Clock to Q
- **High Speed System Design Features**
  Self-timed Write Pulse Generation
  Transparent Output Latch
  Separate Data Input & Output Pins
- **Full Military Temperature Range**
- **Pin Compatible with Insustry Standard**
  MCM6292/5
- **OE for Asynchronous Operation (SSM7195)**
- **28-Pin DIP and SOJ Packages**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

The SSL7192 and SSL7195 ar 65,536-bit synchronous static RAMs organized as 16,384 words by 4 bits. These devices integrate input registers, high speed SRAM array, and output latcheds on the same monolithic chip. The SSM7195 comes with Output Enable control. The synchronous nature of the design allows more precise timing control (such as cycle time) with the use of an external clock (K). These devices are fabricated using Saratoga's proprietary Bipolar CMOS process known as SABiC (Self-Aligned Bipolar CMOS) to attain very high speed and low power consumption.

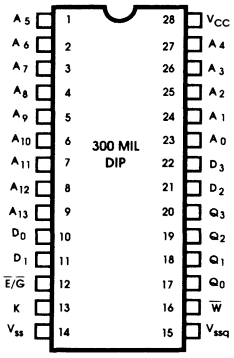
The non-inverting registers for address (A_0-A_{13}), data (D_0-D_3), and write ($\overline{W}$) inputs are clock (K) controlled with positive edge of clock. This simplifies system designer's task as he no longer has to use pulse width for control. As the speed of circuits goes higher, it is extremly difficult to control the pulse width for reliable system operations.

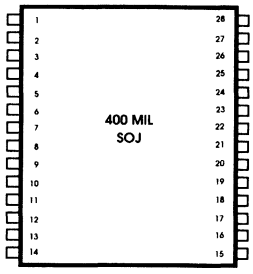
Both the SSM7192 and SSM7195 provide transparent output operation when clock (K) is low for access of RAM data within the same cycle. The output data is latched when (K) is high.

The SSM7195 has an output enable ($\overline{G}$) which provides asynchronous bus control for common I/O and bank switching applications.

Write operations are internally self-timed and initiated by the rising edge of the (K) input. This feature eliminates complex off-chip write pulse generation and provides added flexibility for incoming signals. Both devices will be available in 300 MIL, 28-pin Side Braised and plastic DIPs, and 400 MIL, 28-pin plastic SOJ packages.

PIN CONFIGURATION





Same Pin assignment as DIP

July 1988

FUNCTIONAL BLOCK DIAGRAM

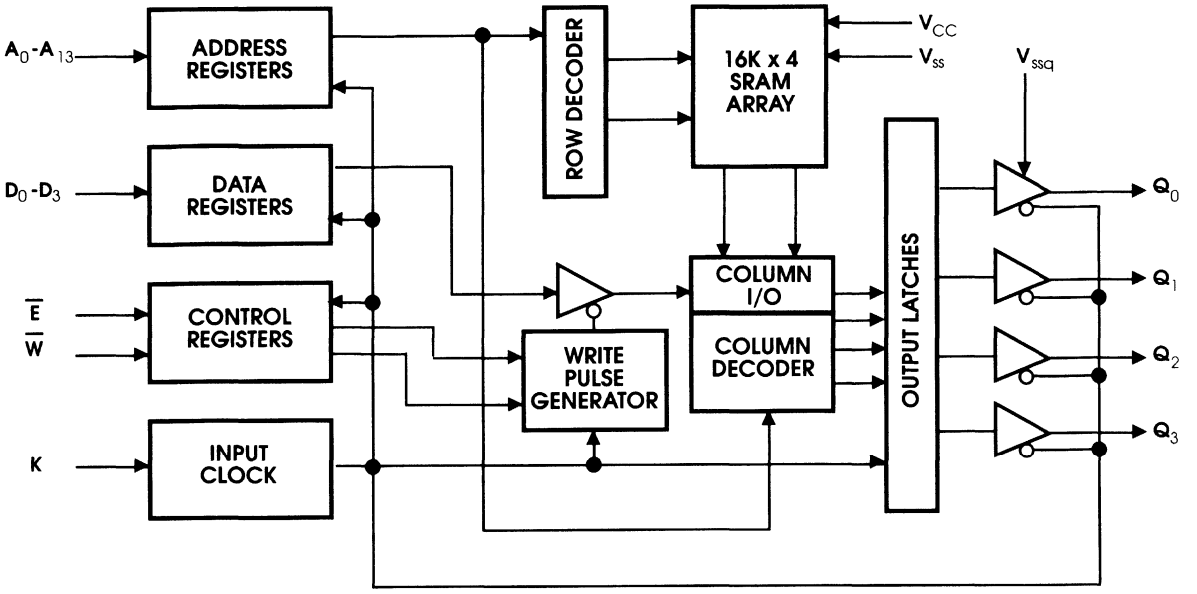


Figure 1: FUNCTIONAL BLOCK DIAGRAM OF SSM7192

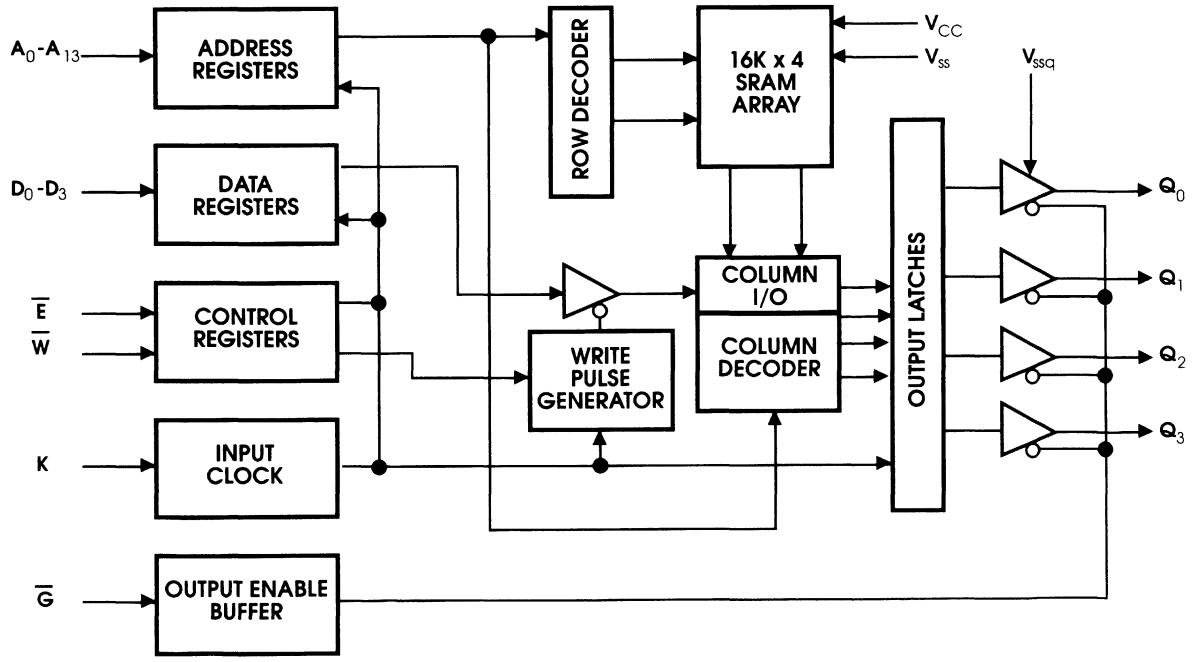


Figure 2: FUNCTIONAL BLOCK DIAGRAM OF SSM7195

Saratoga Semiconductor

SSM7193/4

16K by 4 Bit BiCMOS TTL Synchronous Static RAM
with Output Registers

PRELIMINARY INFORMATION

FEATURES

- **High Performance**
  20ns Access Time
  8ns Clock to Q
- **High Speed System Design Features**
  Self-timed Write Pulse Generation
  Output Registers for Pipelined Operation
  Separate Data Input & Output Pins
- **Full Military Temperature Range**
- **Pin Compatible with Industry Standard**
  MCM6293/4
- **OE for Asynchronous Operation (SSM7194)**
- **28-Pin DIP and SOJ Packages**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

The SSL7193 and SSL7194 ar 65,536-bit synchronous static RAMs organized as 16,384 words by 4 bits. These devices integrate input registers, high speed SRAM array, and output latcheds on the same monolithic chip. The SSM7194 comes with Output Enable control. The synchronous nature of the design allows more precise timing control (such as cycle time) with the use of an external clock (K). These devices are fabricated using Saratoga's proprietary Bipolar CMOS process known as SABiC (Self-Aligned Bipolar CMOS) to attain very high speed and low power consumption.

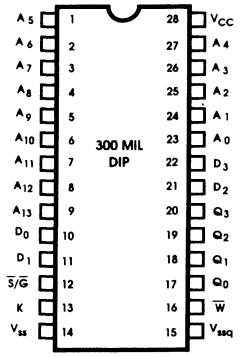
The non-inverting registers for address (A_0-A_{13}), data (D_0-D_3), and write ($\overline{W}$) inputs are clock (K) controlled with positive edge of clock. This simplifies system designer's task as he no longer has to use pulse width for control. As the speed of circuits goes higher, it is extremly difficult to control the pulse width for reliable system operations.

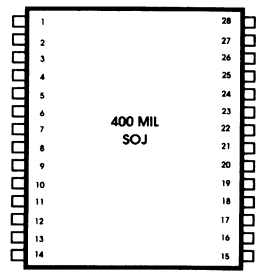
Both the SSM7193 and SSM7194 provide transparent output registers. At the rising edge of the clock (K) data from the previous (K) high cycle is presented at the output pins. This is also called as pipelined operation.

The SSM7194 has an output enable ($\overline{G}$) which provides asynchronous bus control for common I/O and bank switching applications.

Write operations are internally self-timed and initiated by the rising edge of the (K) input. This feature eliminates complex off-chip write pulse generation and provides added flexibility for incoming signals. Both devices will be available in 300 MIL, 28-pin side-braised and plastic DIPs, and 400 MIL, 28-pin plastic SOJ packages.

PIN CONFIGURATION





Same Pin assignment as DIP

Note: V_{SSQ} should be isolated from V_{SS} for low noise applications

July 1988

FUNCTIONAL BLOCK DIAGRAM

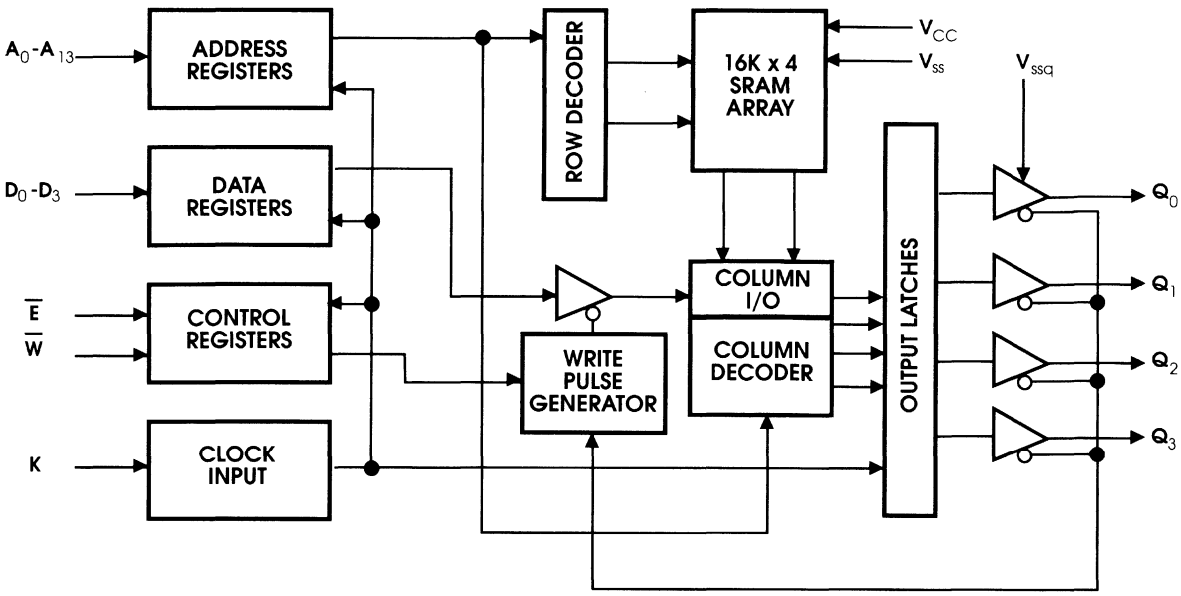


Figure 1: FUNCTIONAL BLOCK DIAGRAM OF SSM7193

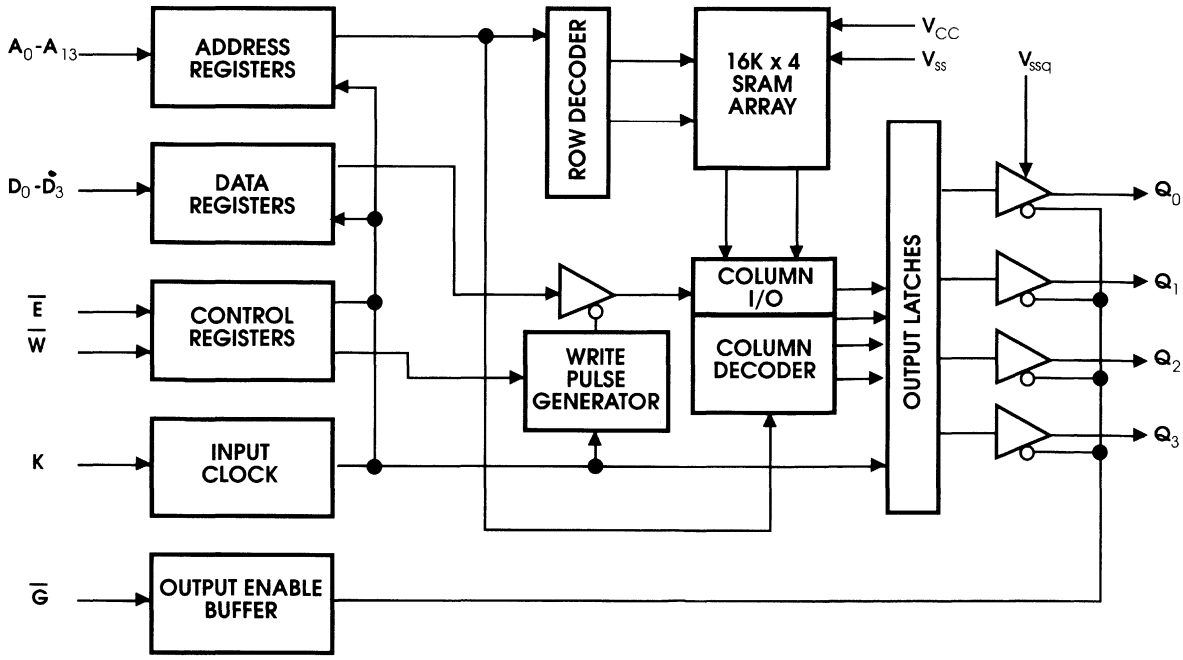


Figure 2: FUNCTIONAL BLOCK DIAGRAM OF SSM7194

BiCMOS TTL CACHE TAGS

Saratoga Semiconductor

SSL4180/1

4K by 4 Bit BiCMOS Cache Tag RAM
ADVANCE INFORMATION

FEATURES

- **Fast Address to MATCH**
  15/20/25/35ns Address to Compare
  13/15/20ns Tag to Compare
- **Flash Clear & Word Width Expandable**
- **Full Military Temperature Range**
- **Industry Standard 22-Pin DIP Packages**
- **Totem-Pole (4180) & Open Drain (4181)**
- **Pin Compatible with MK41H80 & MK4180**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

The SSL4180 & SSL4181 are high performance 16K BiCMOS static RAMs, with a 4K x 4 organization and an on-chip 4-bit comparator. This comparator comapres RAM content and the current input data. The result is active high match on the MATCH (SSL4180) output pin or active low miss on the same pin. The SSL4181 has an active low miss open drain MATCH output. This MATCH output pin can be NAND-ed (in case of SSL4180) or tie-ORed with pull-up resistor (in case of SSL4181).

During READ cycle, the tag data will be transferred from the memory array to the I/O pins (DQ_0 - DQ_3) when the output enable is active ($\overline{OE}$ is low).

An active low Flash Clear signal ($\overline{CLR}$) will clear or reset memory array to all zero. This is used for resetting the tag-ram, flashing it after a miss or for context swithching.

The SSL4180 and SSL4181 are very simple to control. When the Write Enable ($\overline{WE}$) pin is low, a write cycle is initiated. The Output Enable ($\overline{OE}$) pin enables a READ cycle when it is low. The ($\overline{CLR}$) pin enables a Flash Clear cycle when it is low.

The SSL4180/SSL4181 begins a compare cycle with the valid address (refer to Figure 2). A valid MATCH is enabled when ($\overline{OE}$) and ($\overline{WE}$) go high in conjunction with their respective set-up and hold times. MATCH will occur t_{aca} nano-seconds after a valid address, and t_{dca} nano-seconds after valid data in. MATCH will then go invalid t_{ach} nao-seconds after the address changes.

Both devices start a Write cycle with stable addresses (see Figure 2). OE is in "don't care" state. ($\overline{WE}$) may fall with stable addresses, and must remain low until t_{aw} with a duration of t_{wew}. Data in must be held valid t_{ds} nano-seconds before and t nano-seconds after ($\overline{WE}$) goes high. MATCH will be invalid during this entire cycle.

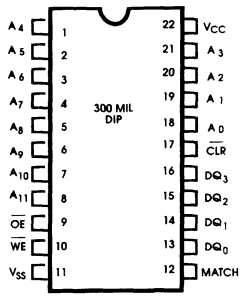
The SSL4180/81 begins a READ cycle with stable addresses and ($\overline{WE}$) high (see Figure 3). DQ becomes valid t_{aa} nano-seconds after valid address, and t_{oea} nano-seconds after the fall of ($\overline{OE}$). The DQ outputs become invalid t_{oh} nano-seconds after the address become invalid or t_{oez} nano-seconds after ($\overline{OE}$) is brought high. Ripple through data access may be accomplished by holding ($\overline{OE}$) active low whil strobing addresses (A_0 - A_{11}), and holding ($\overline{CLR}$) and ($\overline{WE}$) high. The MATCH output will be invalid during the READ cycle.

A Flash Clear Cycle begins as ($\overline{CLR}$) is brought low (see Figure 4). This results in clearing all 16,384 bits of memory to all zero. Control inputs will not be recognized from t_{cx} nano-seconds after ($\overline{CLR}$) falls to t_{cr} after ($\overline{CLR}$) is brought high. ($\overline{OE}$) and ($\overline{WE}$) are "don't cares" and DQ is high Z. MATCH will be invalid as long as ($\overline{CLR}$) is low.

The SSL4180 is pin compatible to Mostek's MK41H80 device.

July 1988

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM

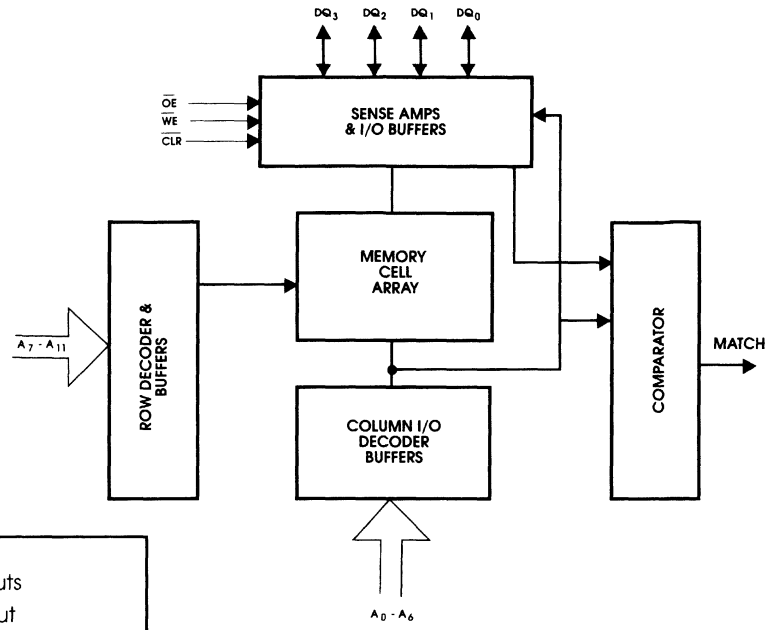


FIGURE 1. Block Diagram

PIN IDENTIFICATION

A_0 - A_{11}	Address Inputs
DQ_0 - DQ_3	Data Inputs/Outputs
MATCH	Comparator Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CLR}$	Flash Clear
V_{CC}	Power (+5V)
V_{SS}	Ground

* Totem-pole for SSL4180 and Open Drain for SSL4181

TRUTH TABLE (X = "DON'T CARE)

WE	OE	CLR	MATCH	MODE
H	H	H	Valid	Compare Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle

ABSOLUTE MAXIMUM RATINGS

Voltage on any Termainal relative to V	-1.0V to +7.0V
Operating Temperature T (Ambient)	0 °C to +70 °C
Storage Temperature (Ceramic)	-65 °C to +150 °C
Storage Temperature (Plastic)	-565 °C to +125 °C
Power Dissipation	1 Watt
Output Current per Pin	50 mA

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data book.

SWITCHING CHARACTERISTICS

SYMBOL	PARAMETER	SSL4180/1-15		SSL4180/1-20		SSL4180/1-25		SSL4180/1-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_c	Cycle Time	20		20		20		20		ns
t_{ccs}	Compare Command Set Up Time	7		7		7		7		ns
t_{cch}	Compare Command Hold Time	0		0		0		0		ns
t_{rcs}	Read Command ($\overline{WE}$) Set Up Time	0		0		0		0		ns
t_{rch}	Read Command ($\overline{WE}$) Hold Time	0		0		0		0		ns
t_{as}	Address Set Up Time	0		0		0		0		ns
t_{aw}	Address Stab;e to End of Write Command ($\overline{WE}$)	12		12		12		12		ns
t_{ah}	Address Hold Time after End of Write	0		0		0		0		ns
t_{wew}	Write Command ($\overline{WE}$) to End of Write	12		12		12		12		ns
t_{ds}	Data Set Up Time	10		10		10		10		ns
t_{dh}	Data Hold Time	0		0		0		0		ns
t_{dca}	Data Compare Access Time (NOTE 4)		13		13		13		13	ns
t_{aca}	Address Compare Access Time (NOTE 4)		15		15		15		15	ns
t_{ach}	Address Compare Hold Time (NOTE 4)	5		5		5		5		ns
t_{dch}	Data Compare Hold Time (NOTE 4)	3		3		3		3		ns
t_{oea}	Output Enable ($\overline{OE}$) Access Time (NOTE 4)		10		10		10		10	ns
t_{oh}	Valid Data Out (DQ) Hold Time (NOTE 4)	5		5		5		5		ns
t_{aa}	Address Access Time (NOTE 4)		20		20		20		20	ns
t_{oez}	Output Enable ($\overline{OE}$) to HIGH Z (NOTE 5)		7		7		7		7	ns
t_{oel}	Output Enable ($\overline{OE}$) to LOW Z (NOTE 5)	2		2		2		2		ns
t_{wez}	Write Enable (WE) to HIGH Z (NOTE 5)		8		8		8		8	ns
t_{wel}	Write Enable ($\overline{WE}$) to LOW Z (NOTE 5)	3		3		3		3		ns

AC ELECTRICAL CHARACTERISTICS (0 °C ≤ T_A ≤ +&) °C) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	SSL4180/1-15		SSL4180/1-20		SSL4180/1-25		SSL4180/1-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{fcc}	Flash Clear Cycle Time	70		70		70		70		ns
t_{cx}	Clear (CLR) to Input "Don't Care"	0		0		0		0		ns
t_{cr}	End of Clear (CLR) to Input Recognized	0		0		0		0		ns
t_{clp}	Flash Clear (CLR) Pulse Width	65		65		65		65		ns

SWITCHING CHARACTERISTICS (CONTINUED)

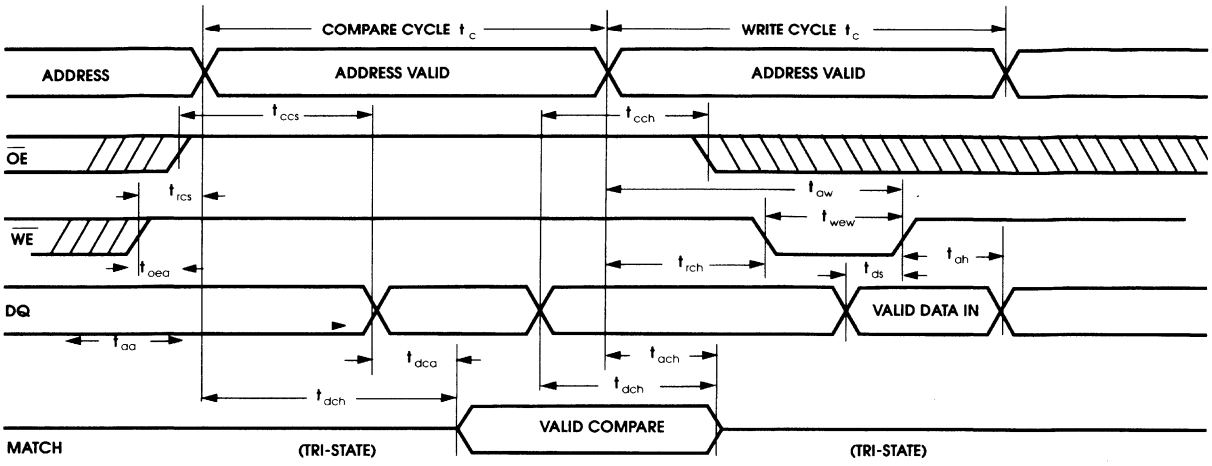


Figure 2. Compare and Write Cycle

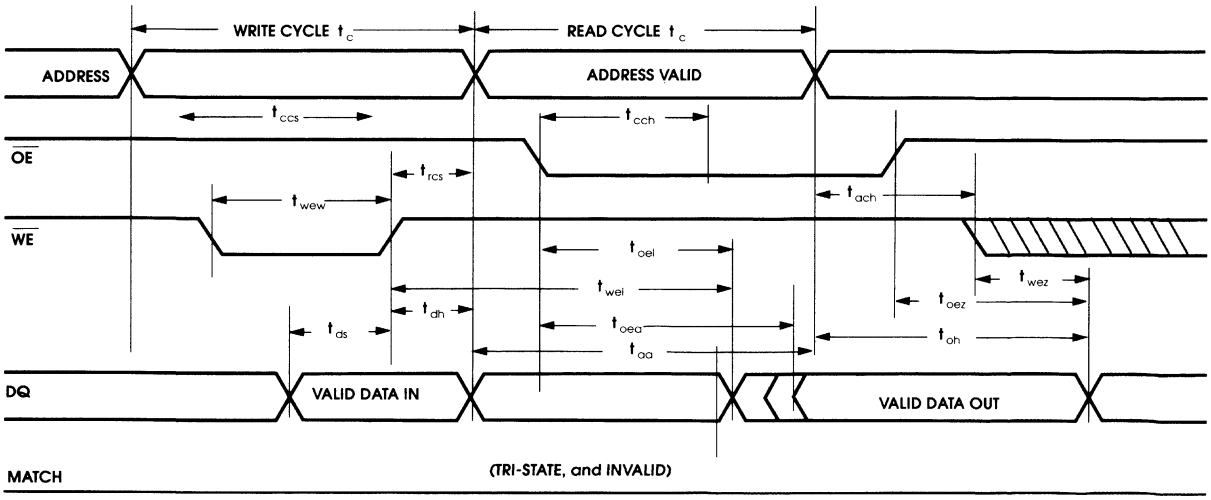
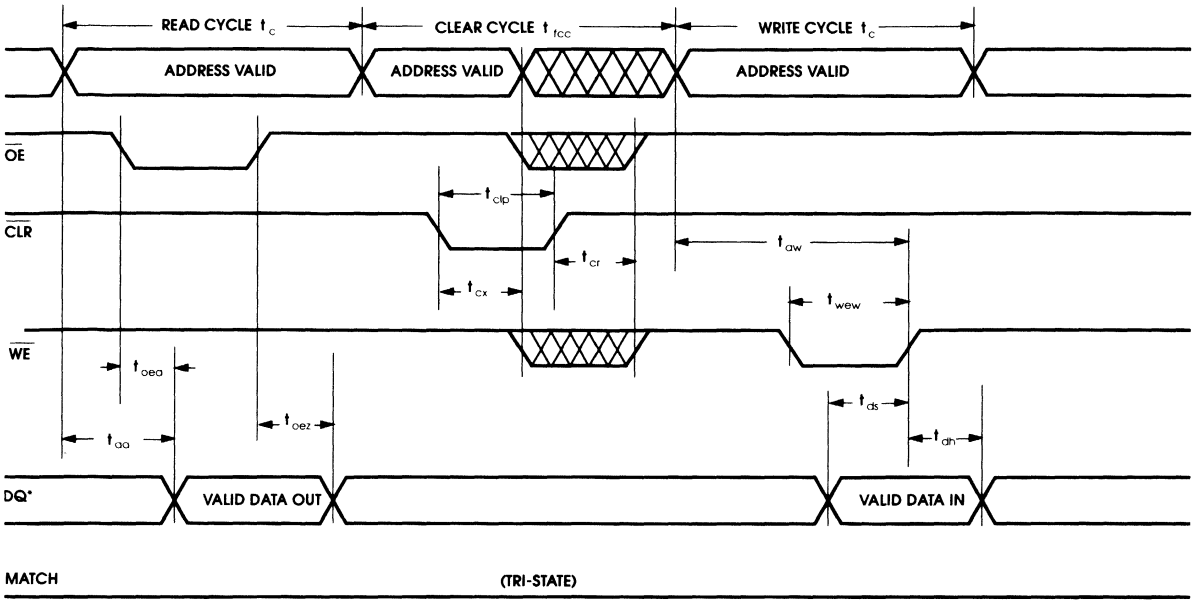


Figure 3. Write and Read Cycle

SWITCHING CHARACTERISTICS (CONTINUED)



*Avoid metastable inputs

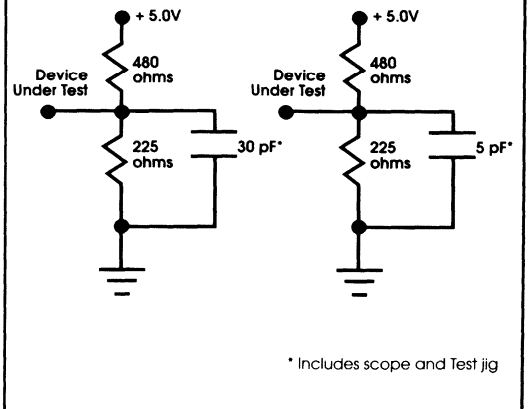
Figure 4. Read-Flash Clear-Write Cycle

AC TEST CONDITIONS

Input Levels	GND to 3.0V
Transition TimesInput & Output Signal Timing	5ns
Reference Level	1.5V
Ambient Temperature	0 °C to +70 °C
V_{CC}	5V ±10%

NOTES:

1. V_{IL} may undershoot to -2.0V for 200ns or less during input transitions.
2. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) with the outputs open circuit. t cycle = minimum duty cycle 100%.
3. Capacities are sampled and not 100% tested.
4. Measured with load shown in Figure 5A.
5. Measured with load shown in Figure 5B.
6. Input leakage current specifications are valid for all DQs such that $0V<V_{OUT}<V_{CC}$. With the exception to MATCH which is always enabled.



* Includes scope and Test jig

Figure 5A & 5B. Ouput Load Circuits

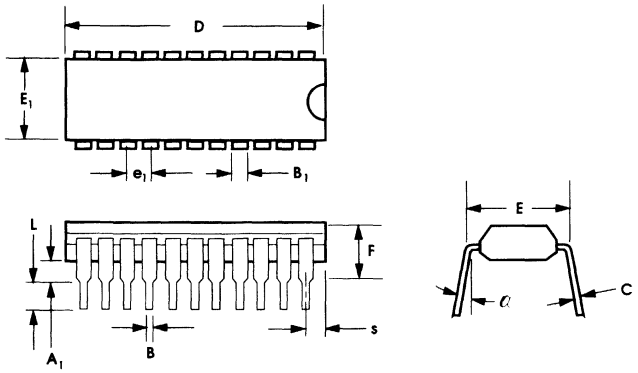
DC ELECRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{CC}	Supply voltage (referenced to V_{ss})	4.5	5.5	V	
V_{SS}	Ground	0.0	0.0	V	
V_{ih}	Input High Voltage, all inputs (referenced to V_{ss})	2.2	V +1	V	
V_{il}	Input Los Voltage, all inputs (referenced to V_{ss})	-1.0	.08	V	1
I_{ccl}	Operating Current (average power supply operating current)		110	mA	2
I_{il}	Input Leakage Current, any input	-10	10	µA	6
I_{ol}	Output Leakage Current	-50	50	µA	
V_{oh}	Output High Voltage, reference to V_{ss} ; I_{oh} = -4 mA	2.4		V	
V_{ol}	Output Low Voltage, reference to V_{ss} ; I_{ol} = +16 mA		0.4	V	

AC ELECRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TYP	MAX	UNIT	NOTE
C_1	Capacitance, on any input pin	4	7	pF	3
C_2	Capacitance, on any output pin	8	10	pF	3

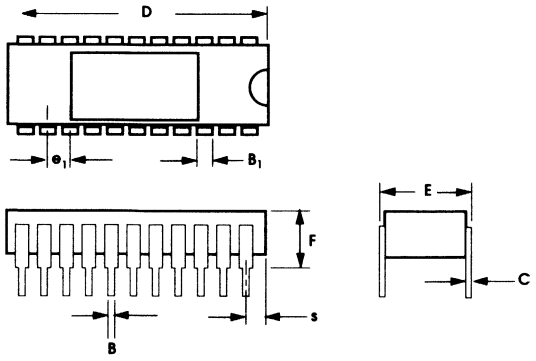
PACKAGE DIMENSIONS



22 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.055
C	.008	.012
D	1.145	1.155
E	.280	.300
E_1	.250	.270
e_1	.090	.110
F		.170
L	.125	.135
s	.070	.080
α	0°	15°

PACKAGE DIMENSIONS



22 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.085	1.115
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

			TEMPERATURE RANGE		
PART NUMBER	SPEED	PACKAGE	MIN	MAX	UNIT
SSL4180-15PC SSL4180-20PC SSL4180-25PC SSL4180-35PC	15ns 20 25 35	22-Pin Plastic DIP	0	+70	°C
SSL4180-15SC SSL4180-20SC SSL4180-25SC SSL4180-35SC	15ns 20 25 35	22-Pin Sidebraze DIP			
SSL4180-20SM SSL4180-25SM SSL4180-35SM	20ns 25 35	22-Pin Sidebraze DIP	-55	+125	°C
SSL4180-15PC SSL4180-20PC SSL4180-25PC SSL4180-35PC	15ns 20 25 35	22-Pin Plastic DIP	0	+70	°C
SSL4180-15SC SSL4180-20SC SSL4180-25SC SSL4180-35SC	15ns 20 25 35	22-Pin Sidebraze DIP			
SSL4180-20SM SSL4180-25SM SSL4180-35SM	20ns 25 35	22-Pin Sidebraze DIP	-55	+125	°C

Saratoga Semiconductor

SSL2152/4

2K by 9 Bit BiCMOS Cache Tag RAM
ADVANCE INFORMATION

FEATURES

- **Fast Address to MATCH**
  20/25/30ns max
- **Full Featured for Design Flexibility**
  On-Chip Parity Generation & Checking
  Parity Error Output & Forced Parity Error Input
  Word Width Expandable
- **Full Military Temperature Range**
- **Industry Standard 28-Pin DIP Packages**
- **Totem-Pole (2152) & Open Drain (2154)**
- **Pin Compatible with TACT2152 & TACT2154**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

The SSL2152 and SSL2154 are 8-bit cache address comparators with on-chip 2K x 9 SRAM array, parity generator, parity checker, and a 9-bit comparator. These two devices are fabricated with the most advanced Saratoga proprietary BiCMOS process with TTL compatible inputs and outputs. Both devices are cascadeable for wider tag address or deeper tag memory size. The SSL2152 has totem-pole MATCH output while the SSL2154 has an open-drain MATCH output for easy OR-tying.

When $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location address by (A_0 - A_{10}) with the (D_0- D_7) plus generated parity. An equality is indicated by a high logic level on the MATCH output pin. A low logic level output on the $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ are low), data on (D_0 - D_7) plus generated odd parity are written into a 9-bit memory location addressed by (A_0 - A_{10}). During the write cycle, a parity error may be forced by holding $\overline{PE}$ low.

A read operation allows the contents of the RAM to be read at the (D_0 - D_7) pins. The read operation is initiated when $\overline{R}$ and $\overline{S}$ are both low, and $\overline{W}$ is high.

A reset input is provided for initialization. A low state at the $\overline{RESET}$ pin will clear (to all zero) the entire 2K x 9 RAM array (with valid parity), and the MATCH output is forced high.

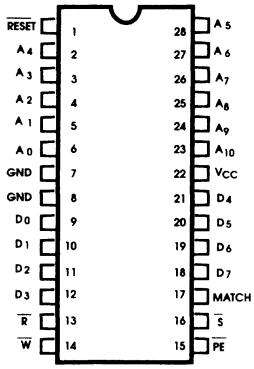
If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high, indicating that the input data, plus generated parity, is equal to the content of that reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a MATCH will not occur unless data has been written into the addressed location. When cascading in the "width" direction, only one bit needs to be tied high regardless of the address size.

Both the SSL2152 and SSL2154 are offered in 28-pin. 600 MIL CERDIP and plastic DIP packages. Products are offered in both commercial and military temperature ranges.

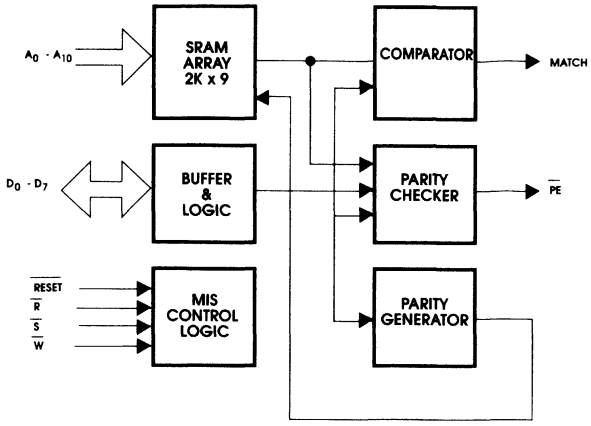
These devices are ideally suited for applications that are based on the Intel, Motorola and other 32-bit RISC micro-processors, with the fastest operating frequencies. With the integrated cache address comparator, the 2K x 9 bits of high speed SRAM, and parity generation and checking capability, the SSL2152 and SSL2154 will reduce chip count, lower system power consumption and shorten design cycle with lower cost.

The simple hand-shaking and controlling features make interfacing to the microprocessors very straight forward.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN IDENTIFICATION

A_0 - A_{10}	Address Inputs
D_0 - D_7	Data Inputs/Outputs
MATCH	Comparator Output
$\overline{RESET}$	Reset
$\overline{R}$	Read Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Control Input
$\overline{PE}$	Parity Error Output/Input
V_{CC}	Power (+5V)
GND	Ground

MATCH OUPUT DESCRIPTION

MATCH = V_{OH} if: $(A_0 - A_{10}) = D_0 - D_7$ + Parity, or $\overline{RESET} = V_{IL}$, or $\overline{S} = V_{IH}$, or $\overline{W} = V_{IL}$

MATCH = V_{OL} if: $(A_0 - A_{10}) \neq D_0 - D_7$ + Parity, with $\overline{RESET} = V_{IH}$, $\overline{S} = V_{IL}$, andr $\overline{W} = V_{IH}$

FUNCTION TABLE

INPUTS				OUTPUTS		I/O	FUNCTIONS
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{RESET}$	Match	$\overline{PE}$	D_0 - D_7	
H	L	L	H	H	H	OUTPUT	
H	H	L	H	L	L	INPUT	READ
				L	H		PARITY ERROR
				H	L		NOT EQUAL
				H	H		UNDEFINED ERROR
L	X	L	H	H	IN	INPUT	EQUAL
X	X	H	H	H	H	HIGH Z	WRITE
X	X	X	L	H	*	*	DEVICE DISABLED
							MEMORY RESET

* THE STATE OF THESE PINS IS DEPENDENT ON INPUTS $\overline{W}$, $\overline{R}$, AND $\overline{S}$.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -1.5V to 7V
Input Voltage Range, any Input ..... -1.5V to 7V
Continuous Power Dissipation 1W
Operating Fre-Air Temperature Range ..... 0 °C to +70 °C
Storage Temperature ..... -65 °C to +150 °C

NOTE: V_{CC} voltage is with respect to ground.

SWITCHING CHARACTERISTICS

(Over Recommended Ranges of Supply Voltage and Operating Temperature))

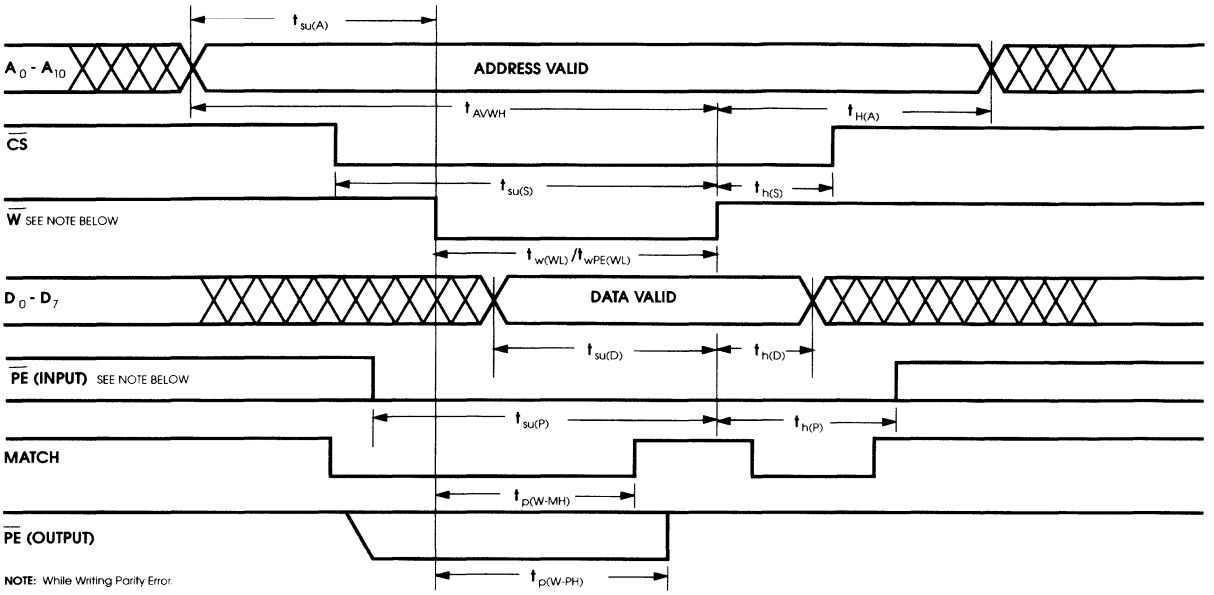
COMPARE CYCLE PARAMETER	SYMBOL	SSL2152/4-20 MIN	TYP	MAX	SSL2152/4-25 MIN	TYP	MAX	SSL2152/4-30 MIN	TYP	MAX	UNIT
Access Time from Address to MATCH	$t_{a(A)}$			20			25			30	ns
Access Time from Address to $\overline{PE}$	$t_{a(A-P)}$			23			28			33	ns
Access Time from $\overline{S}$ to MATCH	$t_{a(S)}$			18			18			20	ns
Prop Delay, Data Inputs to MATCH	$t_{p(D-M)}$			15			17			20	ns
Prop Delay, $\overline{RESET}$ LOW to MATCH HIGH	$t_{p(RST-MH)}$			16			18			21	ns
Prop Delay, $\overline{S}$ HIGH to MATCH HIGH	$t_{p(S-MH)}$			11			12			16	ns
Prop Delay, $\overline{W}$ LOW to MATCH HIGH	$t_{p(W-MH)}$			13			14			17	ns
Prop Delay, $\overline{W}$ LOW to $\overline{PE}$ HIGH	$t_{p(W-PH)}$			12			12			15	ns
MATCH Valid Time after Change of Address	$t_{v(A)}$	6			6			8			ns
MATCH Valid Time after Change of Data	$t_{v(D)}$	2			2			4			ns
MATCH Valid Time (LOW) after S HIGH	$t_{v(S)}$	2			2			4			ns
PE Valid Time after Change of Address	$t_{v(A-P)}$	6			6			8			ns
COMPARE CYCLE PARAMETER											
Read Access Time from Address to D_0 - D_7	$t_{a(A-D)}$			25			30			40	ns
Chip Select Access Time from S LOW to D_0 - D_7	$t_{a(S-D)}$			20			25			35	ns
Prop Delay, $\overline{R}$ LOW to Valid Data Out	$t_{p(R-D)}$			20			25			35	ns
Prop Delay, $\overline{R}$ LOW to MATCH HIGH	$t_{p(R-MH)}$			12			12			15	ns
Prop Delay, $\overline{R}$ LOW to $\overline{PE}$ HIGH	$t_{p(R-PH)}$			12			12			15	ns
Data OUt Disable Time (from HIGH or LOW) (from $\overline{R}$, $\overline{S}$, $\overline{W}$)	t_{dis}			18			20			30	ns
COMPARE CYCLE PARAMETER											
Pulse Duration, $\overline{RESET}$ LOW	$t_{w(RL)}$	40			50			50			ns
Pulse Duration, $\overline{W}$ LOW, w/o Writing $\overline{PE}$	$t_{w(WL)}$	15			15			15			ns
Pulse Duration, $\overline{W}$ LOW, Writing $\overline{PE}$ [1]	$t_{wPE(WL)}$	15			15			15			ns
Address Setup Time Before $\overline{W}$ HIGH	$t_{su(A)}$	0			0			0			ns
Data Setup Time before $\overline{W}$ HIGH	$t_{su(D)}$	10			10			10			ns
$\overline{PE}$ Setup Time before $\overline{W}$ HIGH [1]	$t_{su(P)}$	10			10			10			ns
Chip Select Setup Time before $\overline{W}$ HIGH	$t_{su(S)}$	10			10			10			ns
$\overline{RESET}$ Inactive Setup Time to First Tag Cycle	$t_{su(RH)}$	15			15			15			ns
Address Hold Time after $\overline{W}$ HIGH	$t_{h(A)}$	0			0			0			ns
Data Hold Time after $\overline{W}$ HIGH	$t_{h(D)}$	5			5			5			ns
Data Hold Time after $\overline{W}$ LOW [2]	$t_{h(D-WL)}$	10			10			10			ns
PE Hold Time after $\overline{W}$ HIGH	$t_{h(P)}$	0			0			0			ns
Chip Select Hold Time after W HIGH	$t_{h(S)}$	0			0			0			ns
Address Valid to Write Enable HIGH	t_{AVWH}	15			15			15			ns

[1] Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write Cycle Timing when writing a parity error.

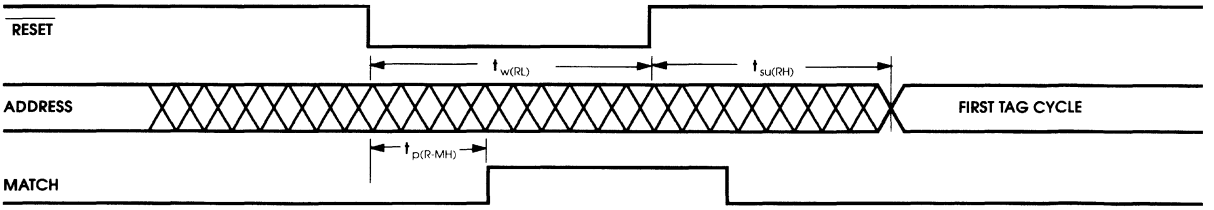
[2] $t_{h(D-HL)}$ guarantees that when $\overline{W}$ is taken low during a compare cycle with MATCH high that match will remain high without a glitch low.

SWITCHING DIAGRAMS

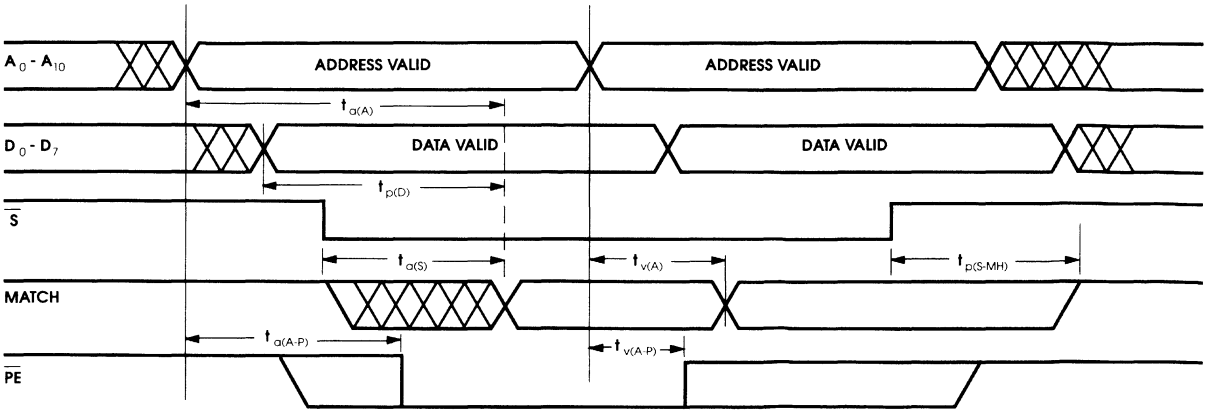
Write Cycle Timing



Reset Cycle Timing

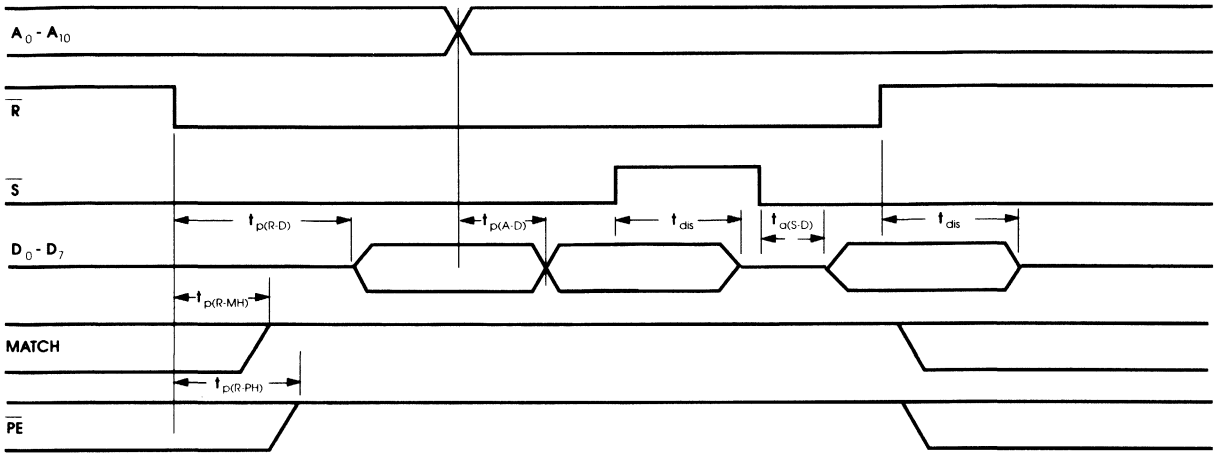


Compare Cycle Timing



SWITCHING DIAGRAMS (CONTINUED)

Read Cycle Timing



AC TEST CONDITIONS

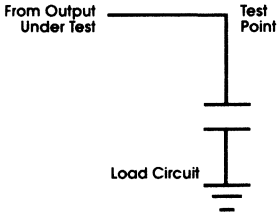


Figure 1. SSL2152 MATCH Output

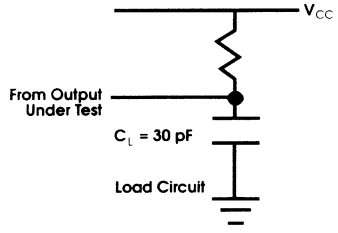


Figure 2. MATCH & PE (O.C.)

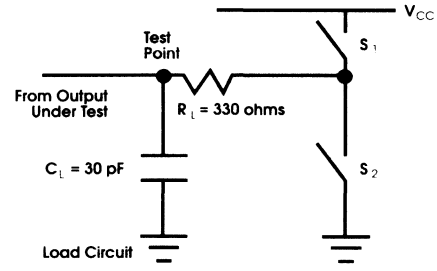


Figure 3. Tri-State Data Outputs

The Following Chart is to be used with Figure 3.

PARAMETER		R_L	C_L	S_1	S_2
t_{en}	t_{pZH}	640 ohms	30 pF	open	closed
	t_{pZL}	640 ohms	30 pF	closed	open
t_{dis}	t_{pHz}	640 ohms	30 pF	open	closed
	t_{pLZ}	640 ohms	30 pF	closed	open
	t_{pd} or t_t	640 ohms	30 pF	open	open

NOTE: C_L includes probe and test fixture capacitance.

RECOMMENDED OPERATING CONDITIONS

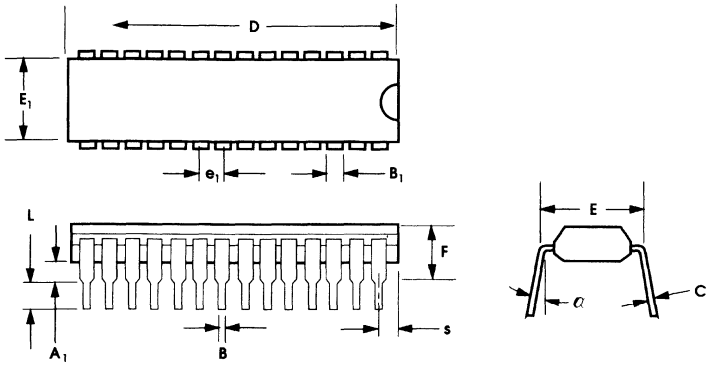
	MIN	TYP	MAX	UNIT
V_{CC}: Supply Voltage	4.5	5.0	5.5	V
V_{IH} : High-Level Input Voltage	2.0		6.0	V
V_{IL} : Low-Level Input Voltage (SEE NOTE BELOW)	-0.5		0.8	V
V_{OH}: High Level Ouput Voltage, MATCH (SSL2154) & PE Output only			5.5	V
I_{OH} : High-Level Output Current, MATCH (SSL2152) & D_0 - D_7			-8.0	mA
I_{OL} : Low-Level Output Current: MATCH (SSL2152)			16	mA
MATCH (SSL2154)-24 mA also available			16	mA
PE - 24 mA also available			16	mA
D_0 - D_7 - 16 mA also available			8.0	mA
T_A : Operating Free-Air Temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (Recommended Free-Air Temperature Range)

PARAMETER		TEST CONDITIONS	SLL2152/54 MIN	TYP	MAX	UNIT
I	Output Leakage Current	CS = V_{IH} ; V_{CC} = max GND ≤ V_{OUT} ≤ V_{CC}	-50		50	mA
V_{OH}	High-Level Output Voltage (2151 MATCH & PE)	I_{OH} = -4mA, V_{CC} = 4.5	2.4			V
V_{OL}	Low-Level Output Voltage, V_{CC} = 4.5V	I_{OL} = 16mA MATCH I_{OL} = 16mA (2152) MATCH I_{OL} = 16mA, PE I_{OL} = 8mA, D_0 - D_7			0.4	V
I_I	Input Current	V_I = 0-V_{CC} ,V_{CC} = 5.5V			10	µA
I_{OS}	Short Circuit Output Current (2152 MATCH)	V_O = GND, V_{CC} = 5.5V	50		150	mA
I_{CC1}	Supply Current (Operative)	$\overline{RESET}$ = V_{CC} = 5.5V, $\overline{S}$ = 0		85	125	mA
I_{CC2}	Supply Current (Reset)	$\overline{S}$ = $\overline{RESET}$ = 0V, V_{CC} = 5.5V		5	10	mA
I_{CC3}	Supply Current (Deselect)	$\overline{RESET}$ = $\overline{S}$ = V_{CC} = 5.5V		75	105	mA
C_I	Input Capacitance	f = 1 MHz			5	pF
C_O	Output Capacitance	f = 1 MHz			6	pF

1 All typical values are a V_{CC} = 5.0V and T_A = 25 °C.
2Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

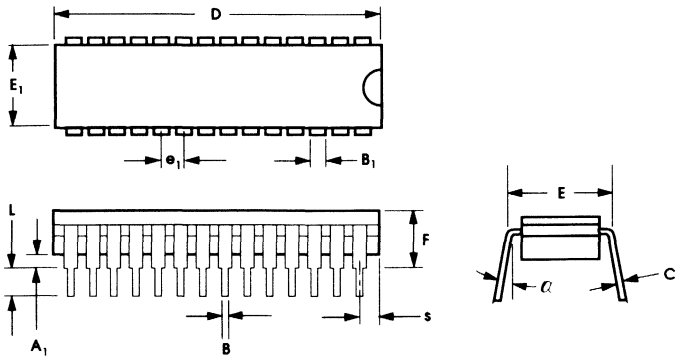
PACKAGE DIMENSIONS



28 LEAD 600 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
	600 MIL	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.055	.065
C	.008	.012
D	1.445	1.455
E	.600	.625
E_1	.530	.550
e_1	.090	.110
F		.190
L	.125	.135
s	.070	.080
α	0°	15°

PACKAGE DIMENSIONS



28 LEAD 600 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.490
E	.590	.620
E_1	.500	.610
e_1	.090	.110
F		.232
L	.125	.200
s		.100
α	0°	15°

ORDERING INFORMATION

			TEMPERATURE RANGE		
PART NUMBER	SPEED	PACKAGE	MIN	MAX	UNIT
SSL2152-20PC SSL2152-25PC SSL2152-30PC	20ns 25 30	28-Pin 600 MIL Plastic DIP	0	+70	°C
SSL2152-20CC SSL2152-25CC SSL2152-30CC	20ns 25 30	28-Pin 600 MIL CERDIP			
SSL2152-25CM SSL2152-30CM	25ns 30	28-Pin 600 MIL CERDIP	-55	+125	°C
SSL2154-20PC SSL2154-25PC SSL2154-30PC	20ns 25 30	28-Pin 600 MIL Plastic DIP	0	+70	°C
SSL2154-20CC SSL2154-25CC SSL2154-30CC	20ns 25 30	28-Pin 600 MIL CERDIP			
SSL2154-25CM SSL2154-30CM	25ns 30	28-Pin 600 MIL CERDIP	-55	+125	°C

BiCMOS TTL FIFOS

Saratoga Semiconductor

SSL7401/2/3/4

64 by 4 and 64 by 5 BiCMOS TTL FIFO Buffer Memory

ADVANCE INFORMATION

FEATURES

- **High Speed Shift-In and Shift-Out**
  10/15/25MHz Cascadeable
  40/50MHz Standalone
- **Full Featured Industry Standard Devices**
  Expandable Word Widths and Depths
  Dual Port RAM Architecture
  Independent Asynchronous Inputs/Outputs
- **Full Military Temperature Range**
- **Output Enable (7403 and 7404)**
- **16 and 18-pin 300 MIL DIP**
- **SABiC BiCMOS Fabrication Technology**
  Fast Bubble-Through Time -16ns
  Fast Data Access Time-15ns
  Fast Setup (0ns) & Hold (5ns) Times

DESCRIPTION

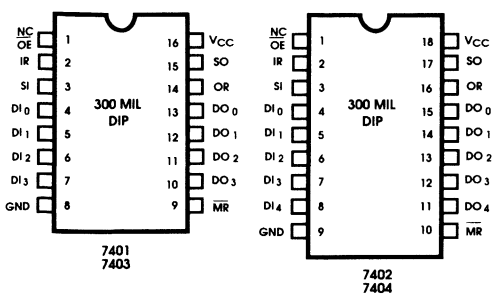
The SSL7401, SSL7402, SSL7403 and SSL7404 are very high performance Parallel First-In First-out (FIFO) memories with asynchronous input and output data rates, making them ideal for applications as data buffers between two digital systems of differing operating speeds. The 50MHz data rate is ideal for analog-to-digital converter buffering and high speed telecommunications and data communications controller applications. The FIFOs are organized as 64 x 4 bits and x 5 bits respectively. All four devices are available in various speeds and configurations per the ordering information chart on the last page.

The combined attributes of low power consumption and high speed are derived from Saratoga's proprietary "Self Aligned Bipolar CMOS," SABiC process technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in speed and density.

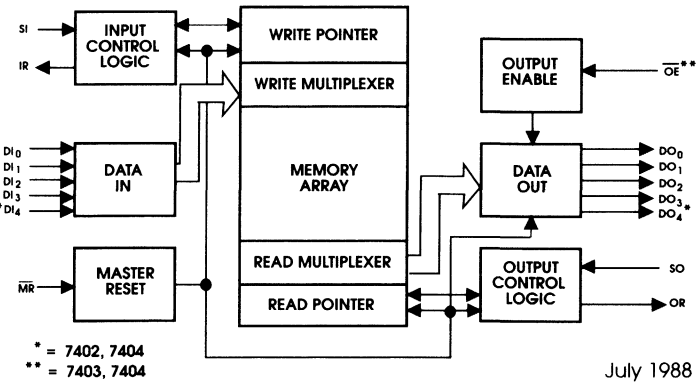
Data is shifted into the FIFO through the four or five bit Data Input pins (DI_0 - $DI_{3/4}$) on the rising edge of the Shift In (SI) signal. The input Ready (IR) output signal indicates whether or not the FIFO is full after every HIGH to LOW SI transition. HIGH indicates the FIFO is not full and ready for more data. Data is shifted out of the FIFO in the same order as it entered, through the four or five bit Data Output pins (DO_0 - $DO_{3/4}$) when the Shift Out (SO) signal is LOW. The Output Ready (OR) signal indicates whether or not the Data Outputs are valid while SO is LOW. OR remains LOW until the data is valid. The data is not valid when the FIFO is empty or data has not propagated to the outputs.

With the Master Reset ($\overline{MR}$) input LOW, the FIFO is reset and the Data Output pins are driven to a logic LOW state, $\overline{IR}$ is driven HIGH and OR is driven LOW. The Output Enable ($\overline{OE}$) input available on the SSL7403 and SSL7404 forces the Data Output to HIGH impedence states when it is at a logic HIGH state. When it is LOW and therefore active, it is used to enable the Data Output pins. The SSL7401/3 are available in 300 MIL, 16-pin DIP and the SSL7402/4 in 300 MIL, 18-pin DIP.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



July 1988

SELECTION GUIDE

		7401/2/3/4 -10	7401/2/3/4 -15	7401/2/3/4 -25	7401/2/3/4 -40*	7401/2/3/4 -50*
Maximum Shift Rate (MHz)		10	15	25	40	50
Maximum Operating Current (mA)	Commercial	70	70	70	75	TBD
	Military	85	85	85	90	TBD

*Speed grades not available for cascadeable version. Only available in Stand-Alone (S) mode (see ordering information).

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65 °C to + 150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in HIGH Z State	-0.5V to +7.0V
DC Input Voltage	-0.8V to +7.0V
Power Dissipation	1.0W
Output Current, into Outputs (LOW)	50mA
Static Discharge Voltage (per MIL-STD 883 Method 3015.2)	>2001V
Latch-Up Current	>200mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0 °C to +70 °C	5V ± 10%
Military	-55 °C to +125 °C	5V ± 10%

ELECTRICAL CHARACTERISTICS (Over Operating Range, unless Otherwise Noted)

PARAMETERS	DESCRIPTION	TEST CONDITIONS		SSL740X- 10, 15, 25, 40, 50 MIN	SSL740X- 10, 15, 25, 40, 50 MAX	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			-0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = max		-10	+10	µA
I_{OS}	Output Short Circuit Current (1)	V_{CC} = Max, V_{OUT} = GND			-150	mA
I_{OZ}	Output Leakage Current	OE = V_{IH}, V_{CC} = max GND ≤ V_{OUT} ≤ V_{CC}		-50	50	µA
I_{CC} (2)	Power Supply Current	OE = V_{IL}, V_{CC} = max Output Open, f = 40 MHz	Commercial		75	mA
			Military		90	mA

CAPACITANCE (2)

PARAMETERS	DESCRIPTION	TEST CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	pF

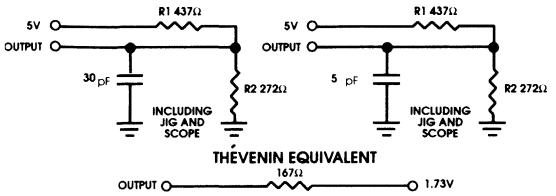
Notes: [1] For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
[2] Tested on sample basis

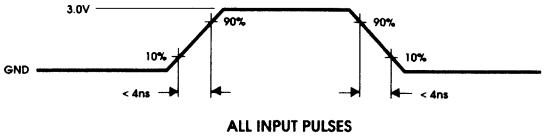
SWITCHING CHARACTERISTICS Over the Operating Range

PARAMETER	DESCRIPTION	TEST CONDITIONS	SSL740X -10		SSL740X -15		SSL740X -25		SSL740X -40*		SSL740X -50*		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_0	Operating Frequency			10		15		25		40		50	MHz
t_{ACC}	Data Access Time	Note 5		45		35		25		17		15/17	ns
t_{PHSI}	SI HIGH Time		20		20		11		7		5		ns
t_{PLSI}	SI LOW Time	Note 5	30		25		24		14		13/14		ns
t_{SSI}	Data Setup to SI	Note 1	0		0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 1	40		30		20		7		5		ns
t_{DLIR}	Delay, SI HIGH to IR LOW	Note 5		40		35		21		20/22		18/22	ns
t_{DHIR}	Delay, SI LOW to IR HIGH	Note 2		45		40		28		20/22		18/22	ns
t_{PHSO}	SO HIGH Time		20		20		11		7		5		ns
t_{PLSO}	SO LOW Time	Note 5	25		25		24		14		13/14		ns
t_{DLOR}	Delay, SO HIGH to OR LOW	Note 5		40		35		20		20/22		18/22	ns
t_{DHOR}	Delay, SO LOW to OR HIGH	Note 5		55		40		29		21/22		19/22	ns
t_{SOR}	Data Setup to OR HIGH	Note 4	0		0		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		5		5		5		5		5		ns
t_{BT}	Bubblethrough Time	Note 3, 5	5	95	5	65	5	50	5	20	5	16/17	ns
t_{SIR}	Data Setup to IR	Note 4	5		5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 4	30		30		20		10		10		ns
t_{PIR}	Input Ready Pulse HIGH	Note 4	5		5		5		5		5		ns
t_{POR}	Output Ready Pulse HIGH		5		5		5		5		5		ns
t_{PMR}	MR Pulse Width		30		25		25		10		7		ns
t_{DSI}	MR HIGH to SI HIGH	Note 4	35		25		10		5		0		ns
t_{DOR}	MR LOW to OR LOW	Note 5		40		35		35		25		20/22	ns
t_{DIR}	MR LOW to IR HIGH	Note 5		40		35		35		25		20/22	ns
t_{LZMR}	MR LOW to Output LOW	Note 5		40		35		25		25		20/22	ns
t_{OOE}	Output Valid from OE LOW	Note 4		35		30		20		15		10	ns
t_{HZOE}	Output HIGH-Z from OE HIGH	Note 4		30		25		15		12		10	ns

NOTES: [1] t_{SSI} will increase if the shift in signal or Data signal 0 to 3V rise time is greater than 4ns. The minimum value of $t_{SSI} + t_{HSI}$ is 5ns or the Shift In rise time.
[2] Not using Full condition.
[3] t_{BT} equals Shift In Low to Output Ready High after Empty condition, or Shift Out Low to Input Ready High after Full condition.
[4] Sample testing only.
[5] Commercial/Military.

AC TEST LOAD AND WAVEFORMS





OPERATING DESCRIPTION

CONCEPT

Unlike traditional FIFOs these devices are designed using a dual port memory, read and write pointer, and control logic. The read and write pointers are incremented by the Shift Out (SO) and Shift In (SI) respectively. The availablitiy of an empty space to shift in data is indicated by the Input Ready (IR) signal, while the presence of data at the output is indicated by the Output Ready (OR) signal. The conventional concept of bubble through is absent. Instead the delay for input data to appear at the output is the time required to move a pointer and propogate an Output Ready (OR) signal. The Output Enable (OE) signal provides the capability to OR tie multiple FIFOs together on a common bus.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset (MR) signal. This causes the FIFO to enter an empty condition signified by the Output Ready (OR) signal being LOW at the same time the Input Ready (IR) signal is HIGH. In this condition, the data outputs (DO_0 - $DO_{3/4}$) will be in a LOW state.

SHIFTING DATA IN

Data is shifted in on the rising edge of the Shift In (SI) signal. This loads input data into the first word location of the FIFO. On the falling edge of the Shift In (SI) signal, the write pointer is moved to the next word position and the Input Ready (IR) signal goes HIGH indicating the readiness to accept new data. If the FIFO is full, the Input Ready (IR) will remain LOW until a word of data is shifted out.

SHIFTING DATA OUT

Data is shifted out of the FIFO on the falling edge of the Shift Out (SO) signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the Output Ready (OR) signal will go HIGH. If data is not present, the Output Ready (OR) signal will stay LOW indicating the FIFO is empty. Upon the rising edge of Shift Out (SO), the Output Ready (OR) signal goes LOW. Previous data remains on the output until the falling edge of Shift Out (SO).

BUBBLE THROUGH

Two bubble through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the Output Ready (OR) flag goes HIGH indicating valid data at the output.

The second bubble through condition occurs when the device is full. Shifting data out creates an empty location which propagates to the input. After a delay, the Input Ready (IR) flag goes HIGH. If the Shift In (SI) signal is HIGH at this time, data on the input will be shifted in.

APPLICATION OF THE 25-50MHz FIFOs

Application of the Saratoga BiCMOS FIFOs requires attention to characteristics not easily specified in a Datasheet, but necessary for reliable operation under all conditions.

When an empty FIFO is filled with initial information, at maximum "shift in" (SI) frequency, followed by immediate shifting out of the data also at maximum "shift out" (SO) frequency, the designer must be aware of a window of time which follows the initial rising edge of the "output ready" (OR) signal during which the SO signal is not recognized. This condition exists only at high speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full frequency operation, but rather delays the full 25-50 MHz operation until after the window has passed.

There are several implementation techniques to manage the window so that all SO signals are recognized:

1) The first involves delaying SO operation such that is does not occur in the critical window. This can be accomplished by causing a fixed delay "initiated by the SI signal only when the FIFO is empty" to inhibit or gate the SO activity. This, however requires that the SO operation at least temporarily be synchronized with the input SI operation. In synchronous applications, this may well be possible and a valid solution.

2) Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is greater than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Saratoga's FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.

3) The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO from the rising edge of the initial "output ready" (OR) signal. This however involves the requirement that this only occurs on the first occurance of data being loaded into the FIFO from any empty condition and therefore requires the knowledge of "input ready" (IR) and (SI) conditions as well as (SO).

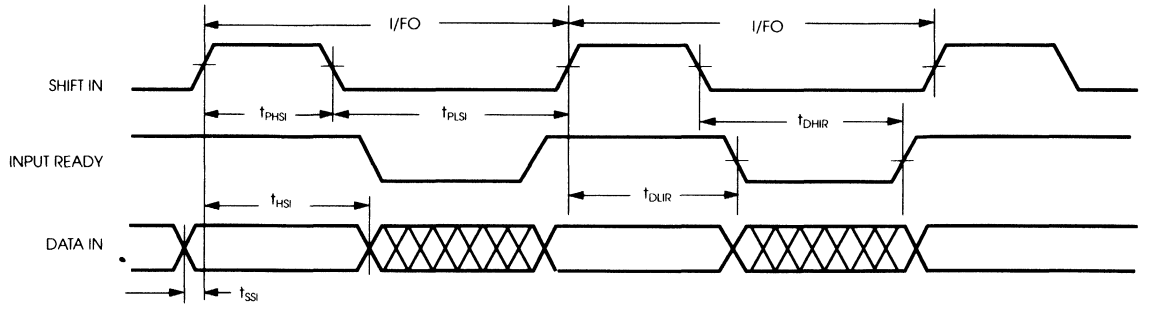
4) Handshaking with the OR signal can be a third method of avoiding the window in question. With this technique, the rising edge of SO, or the fact that the SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken LOW again, advancing the internal pointer to the next data, until the OR signal goes LOW. This assures that the SO pulse that is initiated in the window will be automatically extended sufficient time to be recognized.

5) There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the OR signal is most appropriate because data is guaranteed to be stable prior to and after the OR leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

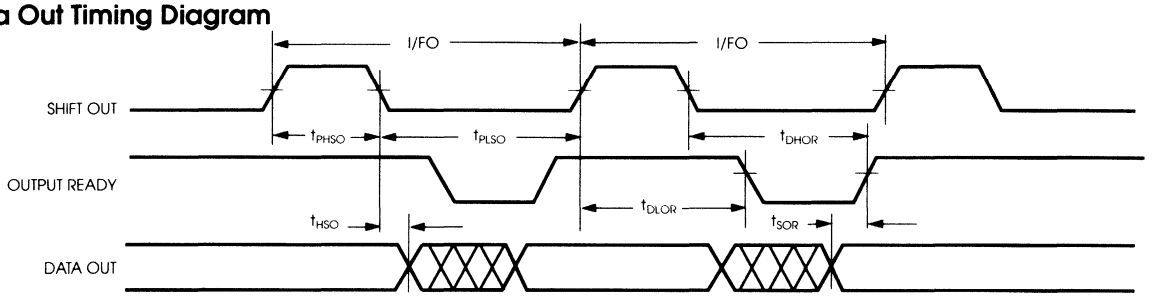
Any of the above solutions will provide a solution for correct operation of a Saratoga FIFO at 25-50 MHz. The specific implementation is left to the designer and dependent on the specific application needs.

SWITCHING WAVEFORMS

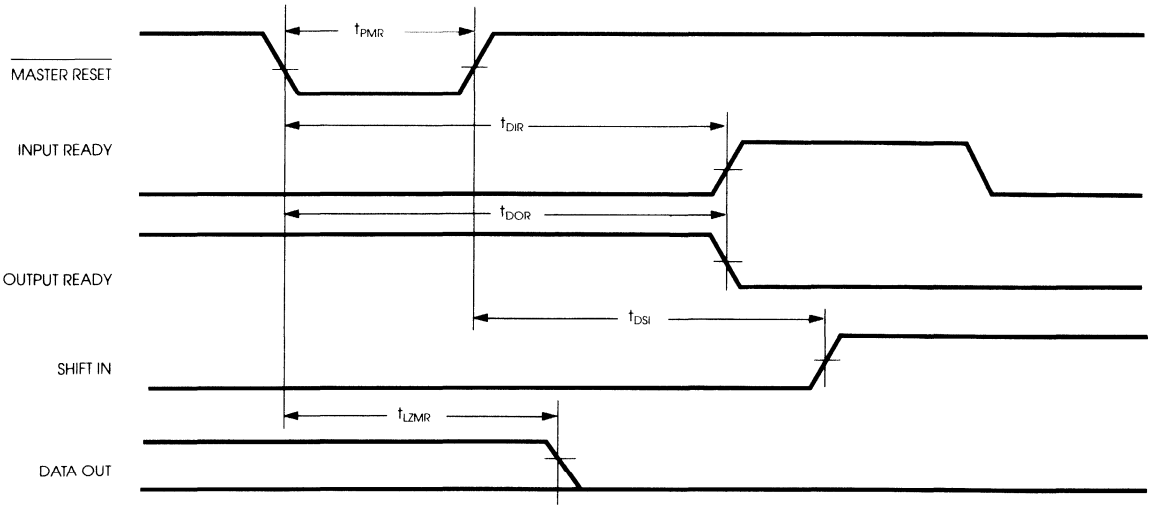
Data In Timing Diagram



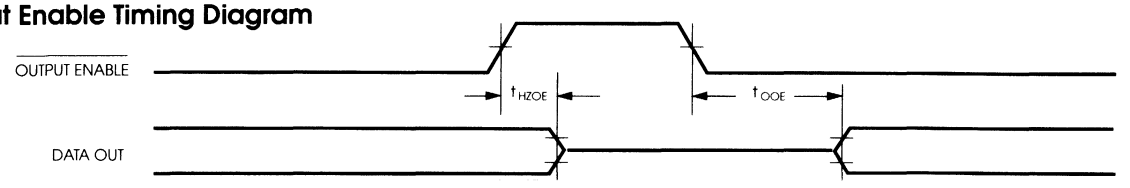
Data Out Timing Diagram



Master Reset Timing Diagram

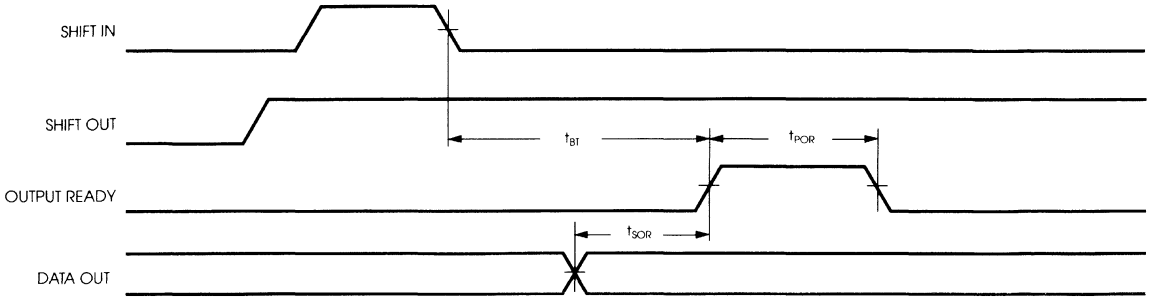


Output Enable Timing Diagram

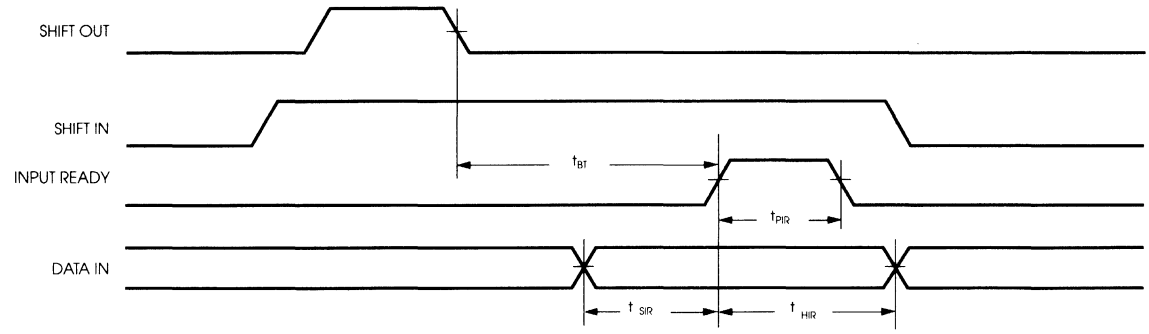


SWITCHING WAVEFORMS (CONTINUED)

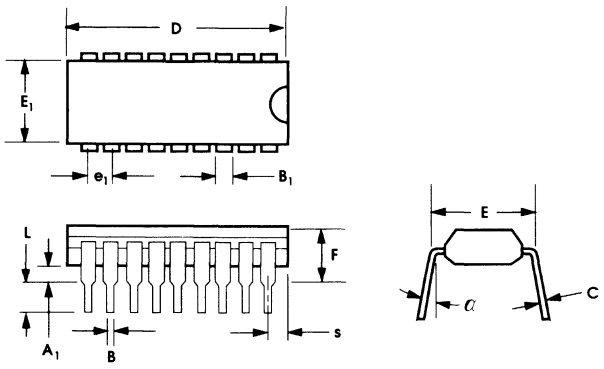
Bubblethrough Data In to Data Out Diagram (Cascadeable)



Bubblethrough, Data Out to Data In Diagram (Cascadeable)



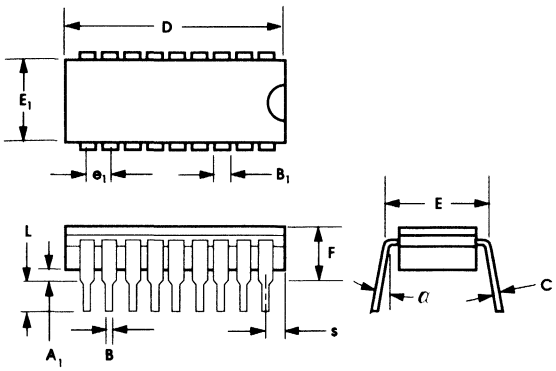
PACKAGE DIMENSIONS



16/18 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	16-PIN		18-PIN	
PARAMETER	MIN	MAX	MIN	MAX
A_1	.015		.015	
B	.016	.020	.016	.020
C	.010	.014	.008	.012
D	.740	.760	.890	.910
E	.280	.300	.280	.300
E_1	.248	.252	.255	.265
e_1	.090	.110	.090	.110
F		.170		.170
L	.125	.145	.125	.135
s	.020	.030	.060	.070
α	0°	15°	0°	15°

PACKAGE DIMENSIONS (CONTINUED)



16/18 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	16-PIN		18-PIN	
PARAMETER	MIN	MAX	MIN	MAX
A_1	.015	.060	.015	.045
B	.014	.023	.014	.023
B_1	.038	.065	.050	.065
C	.008	.015	.009	.015
D		.840		.920
E	.290	.320	.300	.320
E_1	.220	.310	.285	.310
e_1	.090	.110	.090	.110
F		.200		.200
L	.125	.200	.125	.200
s		.080		.080
α	0°	15°	0°	15°

ORDERING INFORMATION

			TEMPERATURE RANGE		
PART NUMBER	SPEED	PACKAGE	MIN	MAX	UNIT
SSL7401S-50PC SSL7401S-40PC SSL7401 -25PC SSL7401 -15PC SSL7401 -10PC	50MHz 40 25 15 10	16-Pin Plastic DIP	0	+70	°C
SSL7401S-50CC SSL7401S-40CC SSL7401 -25CC SSL7401 -15CC SSL7401 -10CC	50MHz 40 25 15 10	16-Pin Ceramic DIP			
SSL7401S-50CM SSL7401S-40CM SSL7401 -25CM SSL7401 -15CM SSL7401 -10CM	50MHz 40 25 15 10	16-Pin Ceramic DIP	-55	+125	°C
SSL7402S-50PC SSL7402S-40PC SSL7402 -25PC SSL7402 -15PC SSL7402 -10PC	50MHz 40 25 15 10	18-Pin Plastic DIP	0	+70	°C
SSL7402S-50CC SSL7402S-40CC SSL7402 -25CC SSL7402 -15CC SSL7402 -10CC	50MHz 40 25 15 10	18-Pin Ceramic DIP			
SSL7402S-50CM SSL7402S-40CM SSL7402 -25CM SSL7402 -15CM SSL7402 -10CM	50MHz 40 25 15 10	18-Pin Ceramic DIP	-55	+125	°C
SSL7403S-50PC SSL7403S-40PC SSL7403 -25PC SSL7403 -15PC SSL7403 -10PC	50MHz 40 25 15 10	16-Pin Plastic DIP	0	+70	°C

ORDERING INFORMATION (CONTINUED)

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSL7403S-50CC SSL7403S-40CC SSL7403 -25CC SSL7403 -15CC SSL7403 -10CC	50MHz 40 25 15 10	16-Pin Plastic DIP			
SSL7403S-50CM SSL7403S-40CM SSL7403 -25CM SSL7403 -15CM SSL7403 -10CM	50MHz 40 25 15 10	16-Pin Ceramic DIP	-55	+125	°C
SSL7404S-50PC SSL7404S-40PC SSL7404 -25PC SSL7404 -15PC SSL7404 -10PC	50MHz 40 25 15 10	18-Pin Plastic DIP	0	+70	°C
SSL7404S-50CC SSL7404S-40CC SSL7404 -25CC SSL7404 -15CC SSL7404 -10CC	50MHz 40 25 15 10	18-Pin Ceramic DIP			
SSL7404S-50CM SSL7404S-40CM SSL7404 -25CM SSL7404 -15CM SSL7404 -10CM	50MHz 40 25 15 10	18-Pin Plastic DIP	-55	+125	°C

Saratoga Semiconductor

SSL7408/9

64 by 8 and 64 by 9 BiCMOS TTL FIFO Buffer Memory

ADVANCE INFORMATION

FEATURES

- **High Speed Shift-In and Shift-Out**
  15/25MHz Cascadeable
  35/40/50MHz Standalone
- **Full Featured Industry Standard Devices**
  Almost Full/Empty and Half Full Flags
  Dual Port RAM Architecture
  Independent Asynchronous Inputs/Outputs
- **Full Military 883C Level Compliant**
- **Output Enable (7408 64 x 8)**
- **28-pin 300 MIL DIP**
- **SABiC BiCMOS Fabrication Technology**
  Fast Bubble-Through Time -16ns
  Fast Flag Speeds -20ns max
  Fast Setup (0ns) & Hold (5ns) Times

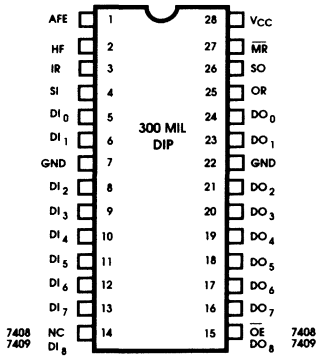
DESCRIPTION

The SSL7408 and SSL7409 are 64-word by 8 and by 9 first-in first-out (FIFO) memories. In addition to the industry standard hand-shaking signals, Almost Full/Almost Empty (AFE) and Half Full (HF) flags are provided. AFE is HIGH when the FIFO is almost full or almost empty. Otherwise, AFE is LOW. HF is HIGH when FIFO is Half full, otherwise HF is LOW. The SSL7408 has an Output Enable (OE) function. The FIFO accepts data inputs (DI_0-DI_8) under the control of Shift-In (SI) signal when the Input Ready (IR) control signal is HIGH. The data is output in the same order as it was stored, on the DO_0-DO_8 output pins under the control of Shift-Out (SO) input when the Output Ready (OR) is HIGH. If the FIFO is full (IR=LOW), pulses at the SI input are ignored. When the FIFO is empty (OR=LOW), pulses at the SO input are ignored.

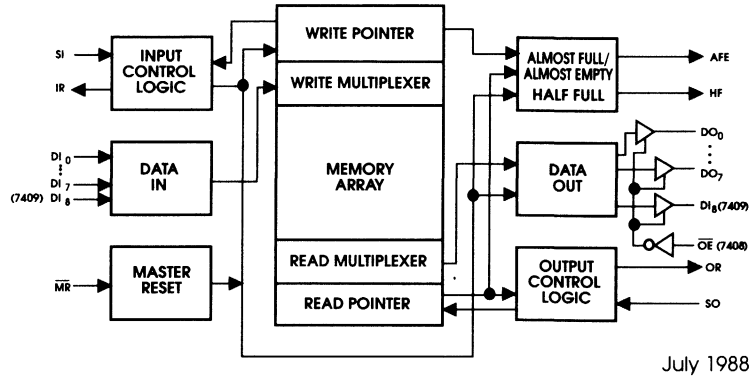
Cascading the FIFOs horizontally (wider word size) or vertically or both can be accomplished via the use of IR and OR pins. Parallel expansion for wider words is done by logically ANDing the IR and OR outputs respectively of individual FIFOs together. This insures that all FIFOs are either ready to accept more data (IR=HIGH) or are ready to output data (OR=HIGH) and thus compensate for variations in propagation delay times between devices. Serial expansion for deeper buffer is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO. Furthermore, to insure proper operation, the SO signal of the upstream FIFO and the IR signal of the downstream FIFO must be connected and the SI signal of the downstream FIFO must be cconnected to the OR output ot the upstream FIFO. In this cascading mode, the IR and OR signals are used to pass data through full and empty FIFOs.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two different digital systems with widely differing operating frequencies. Due to the use of BICMOS technology, these FIFOs attain very high shift-in, shift-out and bubble-through rates. The dual port static RAM architecture further enhances the FIFO performance to satisfy critical needs of data communications and telecommunications applications.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



July 1988

SELECTION GUIDE

		7408-15 7409-15	7408-25 7409-25	7408-35* 7409-35*	7408-40* 7409-40*	7408-50* 7409-50*
Maximum Shift Rate (MHz)		15	25	35	40	50
Maximum Operating Current (mA)	Commercial	110	120	130	135	TBD
	Military	115	125	135	140	TBD

*Speed grades not available for cascadeable version. Only available in Standalone (S) mode (see ordering information).

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65 °C to + 150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in HIGH Z State	-0.5V to +7.0V
DC Input Voltage	-0.8V to +7.0V
Power Dissipation	1.0W
Output Current, into Outputs (Low)	20mA
Static Discharge Voltage (per MIL-STD 883 Method 3015.2)	>2001V
Latch-Up Current	>200mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0 °C to +70 °C	5V ± 10%
Military	-55 °C to +125 °C	5V ± 10%

ELECTRICAL CHARACTERISTICS (Over Operating Range, unless Otherwise Noted)

PARAMETERS	DESCRIPTION	TEST CONDITIONS		SSL7408 SSL7409 MIN	SSL7408 SSL7409 MAX	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16mA			0.4	V
V_{IH}	Input HIGH Voltage	(4)		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage	(4)		-0.5	0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		-10	+10	µA
I_{OS}	Output Short Circuit Current (1)	V_{CC} = Max, V_{OUT} = GND			-150	mA
I_{COQ}	Quiescent Power Supply Current	V_{CC} = Max, I_{OUT} = 0mA; $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$	Commercial		90	mA
			Military		100	mA
I_{CC}(2)	Power Supply Current	$f_{SO} = f_{SI}$ = 40 MHz	Commercial		135	mA
			Military		140	mA

CAPACITANCE(3)

PARAMETERS	DESCRIPTION	TEST CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC}= 4.5V	7	pF

Notes: 1 For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2 $I_{CC} = I_{COQ}$ + 1 mA/MHz (f_{SI}+ f_{SO})/2.
3 Tested on sample basis.
4 For test above 10MHz, this includes any over and under-shoot of the input.

SWITCHING CHARACTERISTICS Over the Operating Range (4)

PARAMETER	DESCRIPTION	TEST CONDITIONS	SSL7408 SSL7409 -15		SSL7408 SSL7409 -25		SSL7408 SSL7409 -35*		SSL7408 SSL7409 -40*		SSL7408 SSL7409 -50*		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_0	Operating Frequency MHz	Note 5		15		25		35		40		50	ns
t_{PHSI}	SI HIGH Time		16		11		9		7		5		ns
t_{PLSI}	SI LOW Time		16		15		14		14		14		ns
t_{SSI}	Data Setup to SI	Note 6	0		0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 6	30		20		12		7		5		ns
t_{DLIR}	Delay, SI HIGH to IR LOW	Note 8		35		21		20/21		19/21		18/21	ns
t_{DHIR}	Delay, SI LOW to IR HIGH	Note 8		40		23		22		20/22		18/22	ns
t_{PHSO}	SO HIGH Time		16		11		9		7		5		ns
t_{PLSO}	SO LOW Time		16		15		14		14		14		ns
t_{DLOR}	Delay, SO HIGH to OR LOW	Note 8		35		21		20/21		19/21		18/21	ns
t_{DHOR}	Delay, SO LOW to OR HIGH	Note 8		40		23		20/21		20/22		18/22	ns
t_{SOR}	Data Setup to OR HIGH		0		0		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		5		5		5		5		5		ns
t_{BT}	Bubblethrough Time	Note 8	8	65	8	50	8	28	8	20	8	16/17	ns
t_{SIR}	Data Setup to IR	Note 7	5		5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 7	30		20		20		10		10		ns
t_{PIR}	Input Ready Pulse HIGH		5		5		5		5		5		ns
t_{POR}	Output Ready Pulse HIGH		5		5		5		5		5		ns
t_{DLZOE}	OE LOW to LOW Z (7408)			35		30		25		15		12	ns
t_{DHZOE}	OE HIGH to HIGH Z (7408)			35		30		25		15		12	ns
t_{DLHHF}	SI toHF HIGH	Note 8		65		55		45		25		18/20	ns
t_{DLHF}	SO to HF LOW	Note 8		65		55		45		25		18/20	ns
t_{DLAFE}	SO or SI to AFE LOW			65		55		45		25		20/22	ns
t_{DHAFE}	SO or SI to AFE HIGH			65		55		45		25		18/23	ns
t_{PMR}	MR Pulse Width		55		45		35		15		7		ns
t_{DSI}	MR HIGH to SI HIGH		25		10		10		5		0		ns
t_{DOR}	MR LOW to OR LOW	Note 8		55		45		35		25		20/23	ns
t_{DIR}	MR LOW to IR HIGH	Note 8		55		45		35		25		20/23	ns
t_{LZMR}	MR LOW to Output LOW	Note 8		55		45		35		25		18/21	ns
t_{AFE}	MR LOW to AFE HIGH			55		45		35		20		15	ns
t_{HF}	MR LOW to HF LOW			55		45		35		20		15	ns
t_{ACC}	Address Access Time			28		20		16/18		16/18		15/17	ns

* Speed grades not available for cascadeable version. Only available in Standalone (S) mode (See ordering information).

NOTES: [4] For test above 10 MHz, this includes any over and under-shoot of the input.

[5] $1/f_O > t_{PHSI} + t_{PLSI}$, $1/f_O > t_{PHSO} + t_{PLSO}$.

[6] t_{SSI} and t_{HSI} apply when memory is not full.

[7] t_{SIR} and t_{HIR} apply when memory is full, SI is HIGH and minimum bubblethrough (t_{BT}) conditions exist.

[8] Commercial/Military

OPERATING DESCRIPTION

SSL7408/9 ARCHITECTURE

The SSL7408 and SSL7409 FIFOs consist of an array of 64 words of 8 or 9-bits each (which are implemented using a dual port RAM cell), a write pointer, a read pointer and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the Almost Full/Almost Empty (AFE) and the Half Full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard SSL7401/402/403/404 FIFOs.

DUAL PORT RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

BUBBLETHROUGH AND FALLTHROUGH

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the Fallthrough time (t_{BT}).

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the Bubble-through time (t_{BT}).

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fallthrough time when it is empty (or near empty) and by the bubble-through time when it is full (or near full).

The conventional definitions of fallthrough and bubble-through do not apply to the SSL7408 and SSL7409 FIFOs because the data is not physically propagated through memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO_0 - DO_8) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

SHIFTING DATA INTO THE FIFO

The availability of an empty location is indicated by the HIGH state of the Input Ready (IR) signal. When IR is HIGH, a LOW to HIGH transition on the Shift-In (SI) pin will load the data on the DI_0 -DI_8 inputs into the FIFO.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH to LOW transition of the SI signal initiates the LOW to HIGH transition of the IR signal, as well as the AFE flag and the HF flag if the FIFO is in the right conditions

SHIFTING DATA OUT OF THE FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the Output Ready (OR) signal. After the FIFO is reset all data outputs (DO$_0$ - DO$_8$) will be in the LOW state. As long as the FIFO remains empty the OR signal will be LOW and all Shift-Out (SO) pulses applied to it will be ignored. After data is shifted into the FIFO, the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse

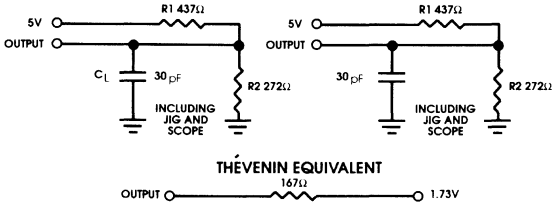
AFE AND HF FLAGS

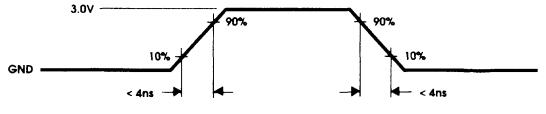
Two flags, Almost Full/Almost Empty (AFE) and Half Full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are eight or less, or 56 or more words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO.

HF	AFE	WORDS STORED
L	H	0 - 8
L	L	9 - 31
H	L	32 - 55
H	H	56 - 64

Flag Definition Table

AC TEST LOAD AND WAVEFORMS

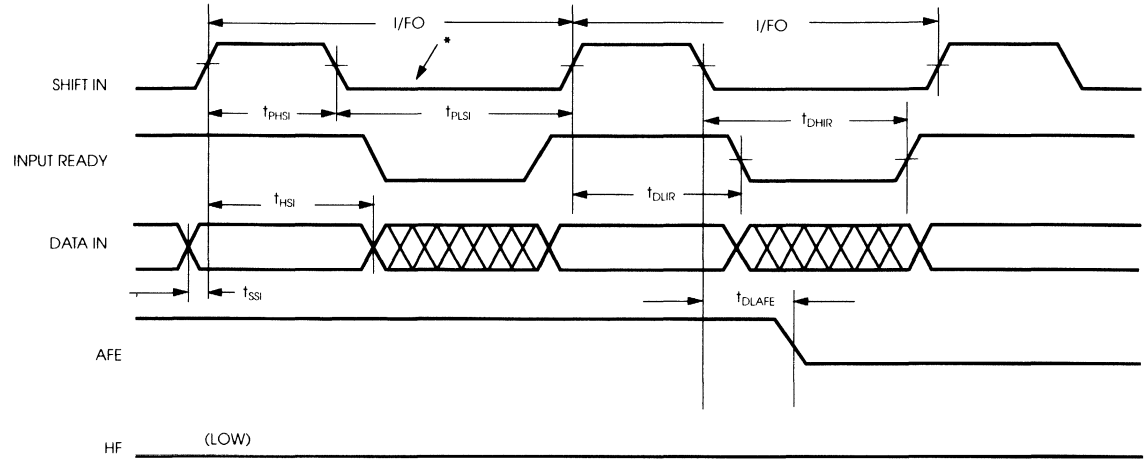




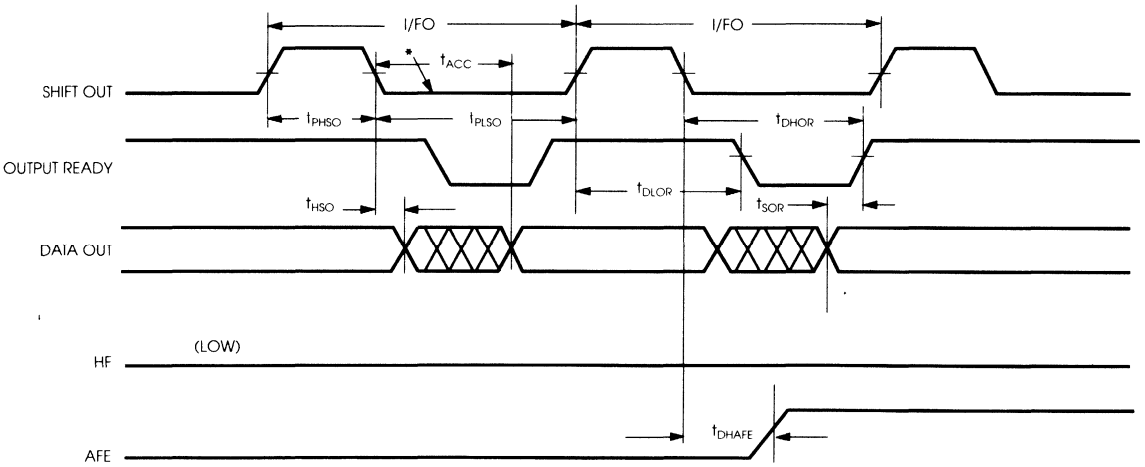
ALL INPUT PULSES

SWITCHING WAVEFORMS

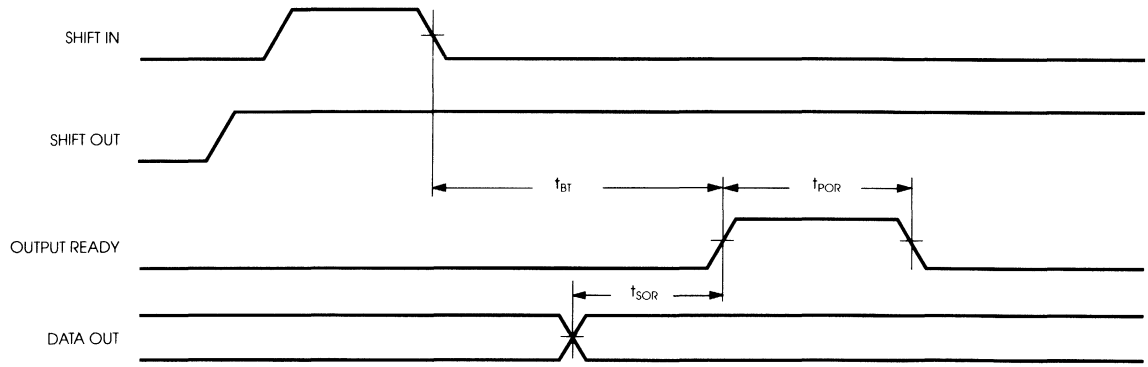
Data In Timing Diagram (FIFO Contains 8 Words)*



Data Out Timing Diagram (FIFO Contains 9 Words)*

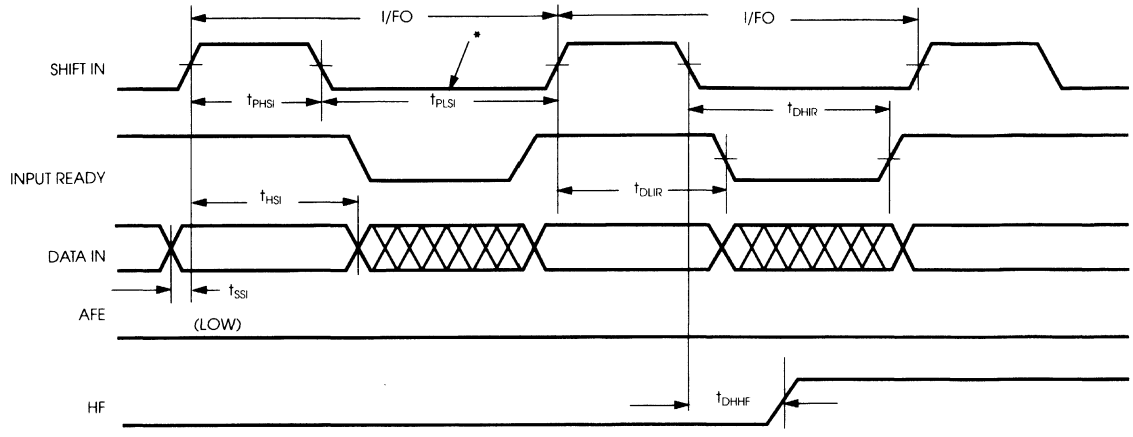


Fallthrough, (Bubblethrough) Data In to Data Out Diagram

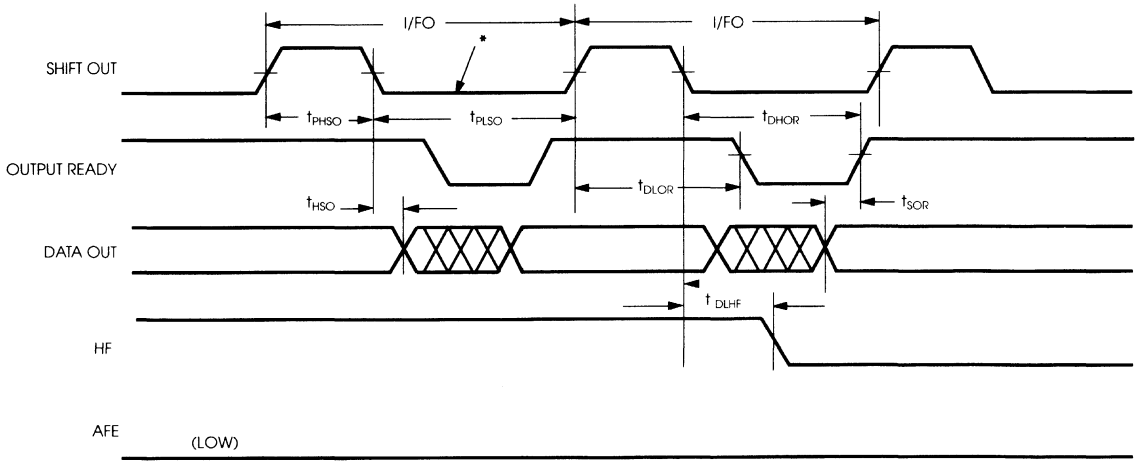


SWITCHING WAVEFORMS (CONTINUED)

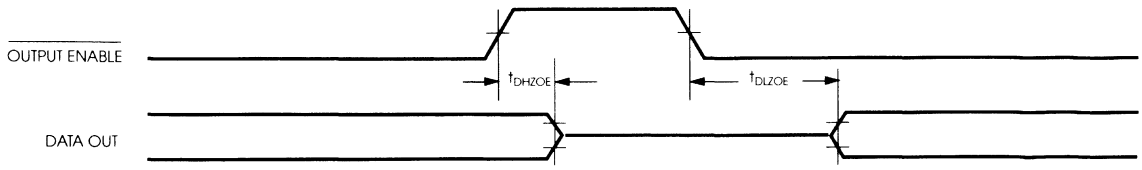
Data In Timing Diagram (FIFO Contains 31 Words)*



Data Out Timing Diagram (FIFO Contains 32 Words)*

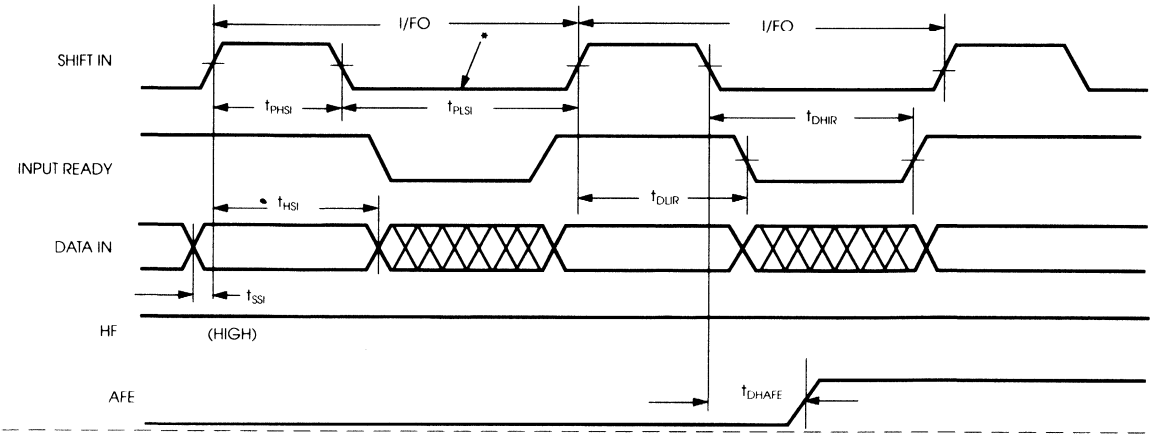


Output Enable Timing Diagram

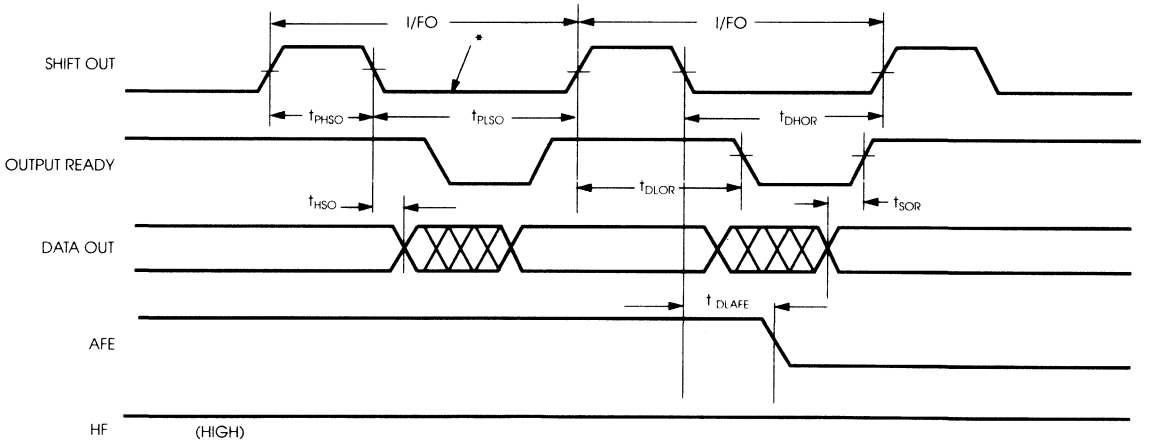


SWITCHING WAVEFORMS (CONTINUED)

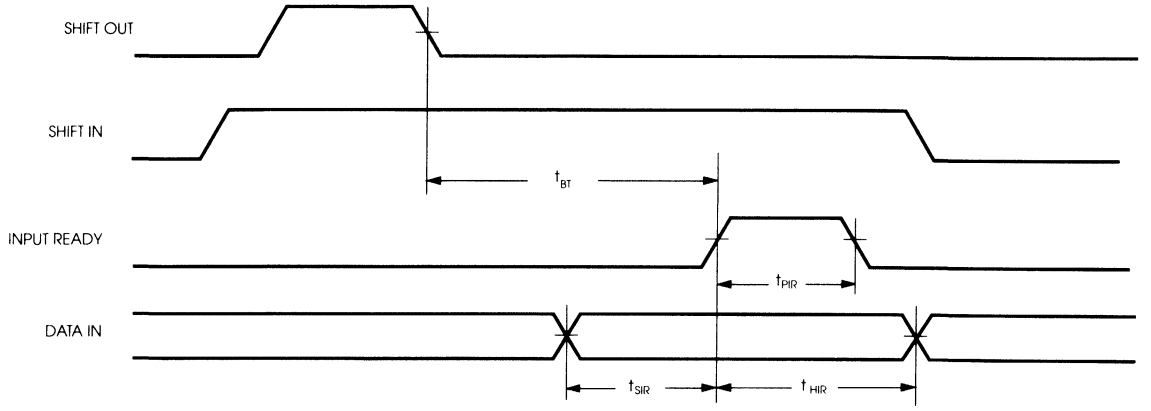
Data In Timing Diagram (FIFO Contains 55 Words)*



Data Out Timing Diagram (FIFO Contains 56 Words)*

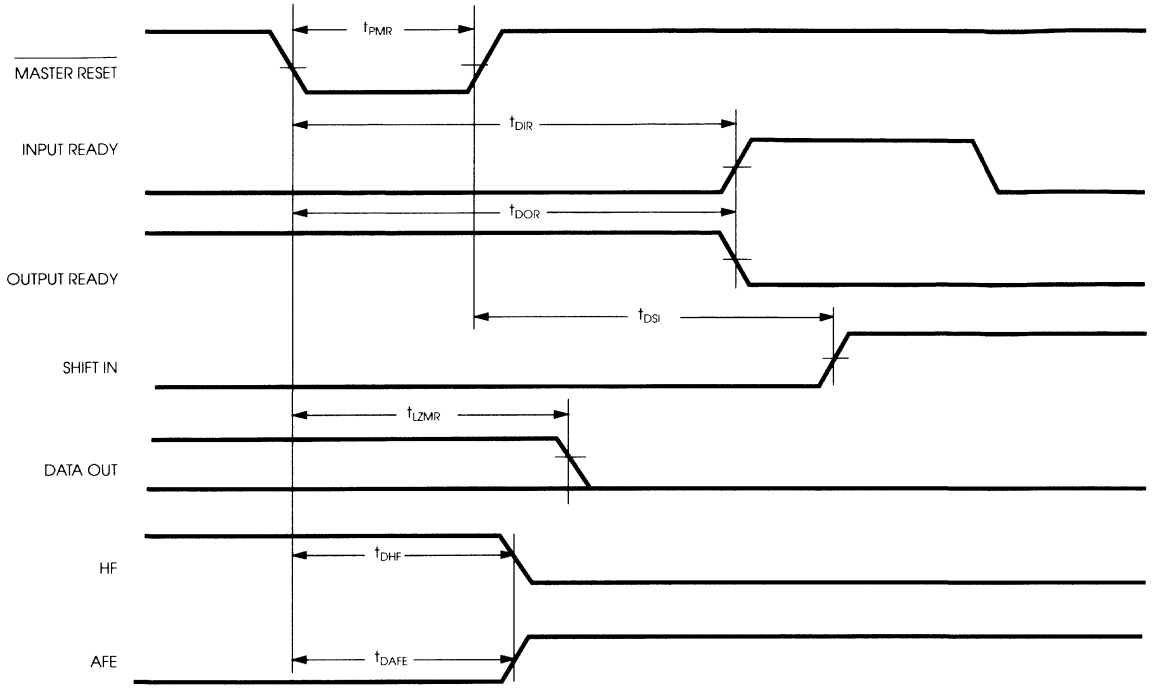


Bubblethrough, Data Out to Data In Diagram

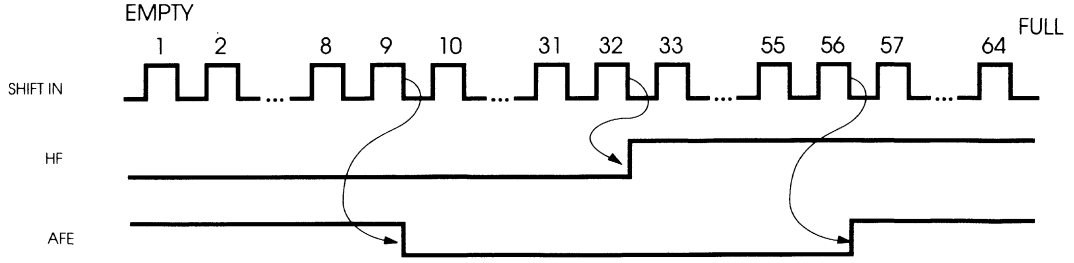


SWITCHING WAVEFORMS (CONTINUED)

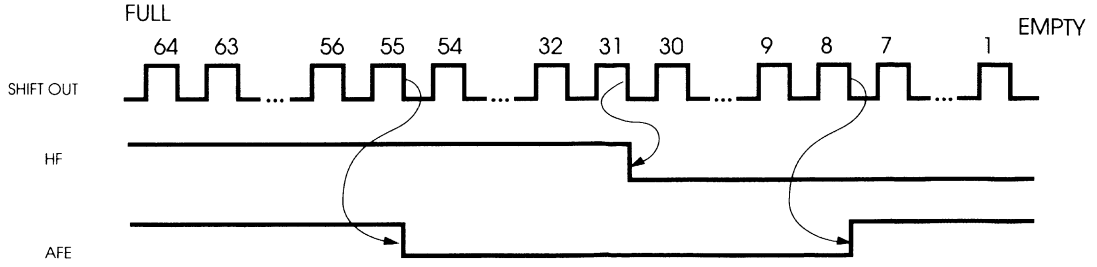
Master Reset Timing Diagram



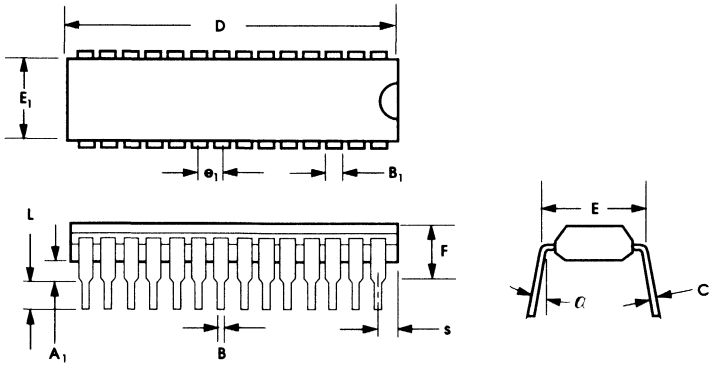
Shifting Words In



Shifting Words Out

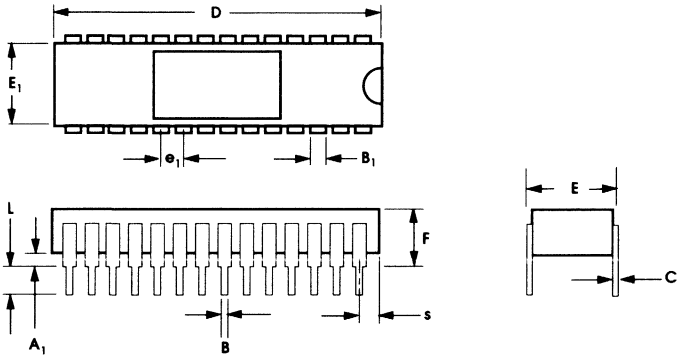


PACKAGE DIMENSIONS (CONTINUED)



28 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	
B	.016	.020
B_1	.045	.055
C	.008	.012
D	1.345	1.355
E	.300	.325
E_1	.270	.290
e_1	.090	.110
F		.170
L	.125	.135
s	.020	.030
α	0°	15°



28 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.385	1.415
E	.285	.305
E_1	.290	.310
e_1	.090	.110
F		.232
L	.125	.200
s		.100

PACKAGE DIMENSIONS (CONTINUED)

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSL7408S-50PC	50MHz	28-Pin Plastic DIP	0	+70	°C
SSL7408S-40PC	40				
SSL7408S-35PC	35				
SSL7408 -25PC	25				
SSL7408 -15PC	15				
SSL7408S-50SC	50MHz				
SSL7408S-40SC	40				
SSL7408S-35SC	35				
SSL7408 -25SC	25				
SSL7408 -15SC	15				
SSL7408S-50SB	50MHz	28-Pin Sidebraze DIP	-55	+125	°C
SSL7408S-40SB	40				
SSL7408 -35SB	35				
SSL7408 -25SB	25				
SSL7408 -15SB	15				
SSL7409S-50PC	50MHz	28-Pin Plastic DIP	0	+70	°C
SSL7409S-40PC	40				
SSL7409S-35PC	35				
SSL7409 -25PC	25				
SSL7409 -15PC	15				
SSL7409S-50SC	50MHz				
SSL7409S-40SC	40				
SSL7409S-35SC	35				
SSL7409 -25SC	25				
SSL7409 -15SC	15				
SSL7409S-50SB	50MHz	28-Pin Sidebraze DIP	-55	+125	°C
SSL7409S-40SB	40				
SSL7409S-35SB	35				
SSL7409 -25SB	25				
SSL7409 -15SB	15				

Saratoga Semiconductor

SSL7413

64 by 5 BiCMOS TTL FIFO Buffer Memory with Status Flags

ADVANCE INFORMATION

FEATURES

- **High Speed Shift-In and Shift-Out**
  15/25MHz Cascadeable
  35/40/50MHz Standalone
- **Full Featured Industry Standard Device**
  Expandable Word Widths and Depths
  Dual Port RAM Architecture
  Independent Asynchronous Inputs/Outputs
- **Full Military Temperature Range**
- **Almost Full/Empty and Half Full Flags**
- **20-pin 300 MIL DIP**
- **SABiC BiCMOS Fabrication Technology**
  Fast Bubble-Through Time -16ns
  Fast Flag Speed - 20ns max
  Fast Setup (0ns) & Hold (5ns) Time

DESCRIPTION

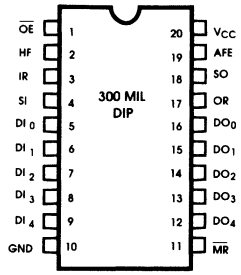
The SSL7413 is a 64-word by 5 bits first-in first-out (FIFO) memory. In addition to the industry standard handshaking signals, Almost Full/Almost Empty (AFE) and Half Full (HF) flags are provided. AFE is HIGH when the FIFO is almost full or almost empty. Otherwise, AFE is LOW. HF is HIGH when the FIFO is Half full, otherwise HF is LOW. The FIFO accepts data inputs (DI_0-DI_4) under the control of Shift-In (SI) signal when the Input Ready (IR) control signal is HIGH. The data is output in the same order as it was stored, on the DO_0-DO_4 output pins under the control of Shift-Out (SO) input when the Output Ready (OR) is HIGH. If the FIFO is full (IR=LOW), pulses at the SI input are ignored. When the FIFO is empty (OR=LOW), pulses at the SO input are ignored.

Cascading the FIFOs horizontally (wider word size) or vertically or both can be accomplished via the use of IR and OR pins. Parallel expansion for wider words is done by logically ANDing the (IR) and (OR) outputs respectively of individual FIFOs together. This insures that all FIFOs are either ready to accept more data (IR = HIGH) or ready to output data (OR=HIGH) and thus compensate for variations in propagation delay times between devices.

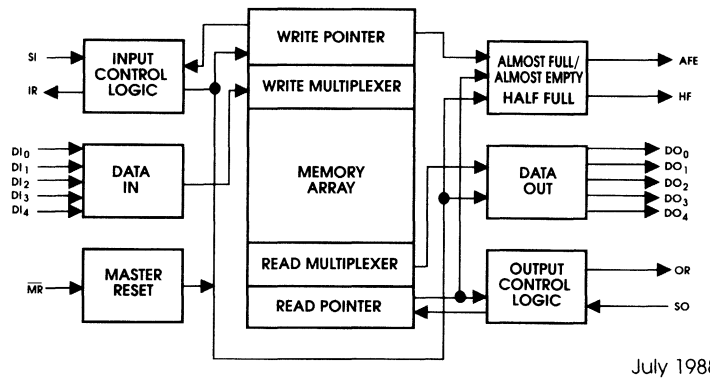
Serial expansion for deeper FIFO words is possible except for the 35, 40 and 50MHz standalone devices. All devices are available in various speeds per the ordering information chart on the last page.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two different digital systems with widely differing operating frequencies. Due to the use of BiCMOS technology, these FIFOs attain very high shift-in, shift-out and bubble-through rates. The dual port static RAM architecture further enhances the FIFO performance to satisfy the critical needs of data communications and telecommunications applications.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



July 1988

SELECTION GUIDE

		7413-15	7413-25	7413-35*	7413-40*	7413-50*
Maximum Shift Rate (MHz)		15	25	35	40	50
Maximum Operating Current (mA)	Commercial	90	90	90	90	TBD
	Military	100	100	100	100	TBD

*Speed grades not available for cascadeable version. Only available in Standalone (S) mode (see ordering information).

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65 °C to + 150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in HIGH Z State	-0.5V to +7.0V
DC Input Voltage	-0.8V to +7.0V
Power Dissipation	1.0W
Output Current, into Outputs (Low)	50mA
Static Discharge Voltage (per MIL-STD 883 Method 3015.2)	>2001V
Latch-Up Current	>200mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0 °C to +70 °C	5V ± 10%
Military	-55 °C to +125 °C	5V ± 10%

ELECTRICAL CHARACTERISTICS (Over Operating Range, unless Otherwise Noted)

PARAMETERS	DESCRIPTION	TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 24mA	Commercial		0.4	V
			Military		0.5	V
V_{IH}	Input HIGH Voltage	(4)		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage	(4)		-0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{OE}$ = V_{IH}, V_{CC}= max. GND ≤V_{OUT}≤V_{CC}		-50	50	µA
I_{OS}	Output Short Circuit Current (1)	V_{CC} = Max, V_{OUT} = GND			-150	mA
I_{COQ}	Quiescent Power Supply Current	V_{CC} = Max, I_{OUT} = 0mA; V_{IN} ≤ OV, V_{IN} ≥ 2V	Commercial		45	mA
			Military		60	mA
I_{CC}(2)	Power Supply Current	f_{SO} = f_{SI} = 40 MHz	Commercial		90	mA
			Military		100	mA

CAPACITANCE (3)

PARAMETERS	DESCRIPTION	TEST CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC}= 4.5V	7	pF

Notes:
1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. I_{CC} = I_{COQ} + 1 mA/MHz* (f_{SI}+ f_{SO})/2.
3. Tested on sample basis.
4. For test above 10MHz, this should include any over and under shoot of the inputs.

SWITCHING CHARACTERISTICS Over the Operating Range (4)

PARAMETER	DESCRIPTION	TEST CONDITIONS	SSL7413 -15		SSL7413 -25		SSL7413 -35*		SSL7413 -40*		SSL7413 -50*		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_0	Operating Frequency MHz	Note 5		15		25		35		40		50	ns
t_{PHSI}	SI HIGH Time		23		16		9		7		5		ns
t_{PLSI}	SI LOW Time	Note 8	25		20		17		14		13/14		ns
t_{SSI}	Data Setup to SI	Note 6	0		0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 6	30		20		10		5		5		ns
t_{DLIR}	Delay, SI HIGH to IR LOW	Note 8		35		28		18/22		18/21		18/21	ns
t_{DHIR}	Delay, SI LOW to IR HIGH	Note 8		40		25		20/22		20/21		19/21	ns
t_{PHSO}	SO HIGH Time		23		16		9		9		5		ns
t_{PLSO}	SO LOW Time	Note 8	25		20		17		14		13/14		ns
t_{DLOR}	Delay, SO HIGH to OR LOW	Note 8		35		28		18/22		18/21		18/21	ns
t_{DHOR}	Delay, SO LOW to OR HIGH	Note 8		40		25		20/22		20/21		19/21	ns
t_{SOR}	Data Setup to OR HIGH		0		0		1		0		0		ns
t_{HSO}	Data Hold from SO LOW		5		5		5		5		5		ns
t_{BT}	Bubblethrough Time	Note 8		60		40		28		20		16/17	ns
t_{SIR}	Data Setup to IR	Note 7	5		5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 7	15		10		10		10		10		ns
t_{PIR}	Input Ready Pulse HIGH		5		5		5		5		5		ns
t_{POR}	Output Ready Pulse HIGH		5		5		5		5		5		ns
t_{DHHF}	SI to HF HIGH			50		40		28		20		18	ns
t_{DLHF}	SO to HF LOW			50		40		28		20		18	ns
t_{DLAFE}	SO or SI to AFE LOW	Note 8		50		40		28		20		20/21	ns
t_{DHAFE}	SO or SI to AFE HIGH	Note 8		50		40		28		20		20/22	ns
t_{PMR}	MR Pulse Width		35		30		25		10		7		ns
t_{DSI}	MR HIGH to SI HIGH		45		35		20		5		0		ns
t_{DOR}	MR LOW to OR LOW	Note 8		35		30		28		25		20/21	ns
t_{DIR}	MR LOW to IR HIGH	Note 8		35		30		28		25		20/22	ns
t_{AFE}	MR LOW to AFE HIGH			35		30		25		20		15	ns
t_{HF}	MR LOW to HF LOW			35		30		25		20		15	ns
t_{ACC}	Address Access Time	Note 8		20		20		20		17		15/17	ns
t_{HZOE}	Output disable from L or H to Z			20		15		12		12		10	ns
t_{DLZOE}	Output enable from Z to L or H			20		20		15		15		10	ns
t_{LZMR}	Reset LOW to Output LOW	Note 8		35		35		25		20		18/20	ns

* Speed grades not available for cascadeable version. Only available in Standalone (S) mode (See ordering information).

NOTES: [4] For test above 10 MHz, this includes any over and under-shoot of the input.

[5] $1/f_O > t_{PHSI} + t_{PLSI}$, $1/f_O > t_{PHSO} + t_{PLSO}$.

[6] t_{SSI} and t_{HSI} apply when memory is not full.

[7] t_{SIR} and t_{HIR} apply when memory is full, SI is HIGH and minimum bubblethrough (t_{BT}) conditions exist.

[8] Commercial/Military

OPERATING DESCRIPTION

SSL7413 ARCHITECTURE

The SSL7413 FIFO consists of an array of 64 words of 5 bits each (which are implemented using a dual port RAM cell), a write pointer, a read pointer and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the Almost Full/Almost Empty (AFE) and the Half Full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard SSL7401/402/403/404 FIFOs.

DUAL PORT RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

BUBBLETHROUGH AND FALLTHROUGH

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the Fallthrough time (t_{BT}).

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the Bubble-through time (t_{BT}).

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fallthrough time when it is empty (or near empty) and by the bubble-through time when it is full (or near full).

The conventional definitions of fallthrough and bubble-through do not apply to the SSL7413 FIFO because the data is not physically propagated through memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst case propagation delay for the control signals. That is, the time required to increment The write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset (MR) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO_0 - DO_4) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

SHIFTING DATA INTO THE FIFO

The availability of an empty location is indicated by the HIGH state of the Input Ready (IR) signal. When IR is HIGH, a LOW to HIGH transition on the Shift-In (SI) pin will load the data on the DI_0 -DI_4 inputs into the FIFO.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH to LOW transition of the SI signal initiates the LOW to HIGH transition of the IR signal, as well as the AFE flag and HF flagn if the FIFO is in the right conditions

SHIFTING DATA OUT OF THE FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the Output Ready (OR) signal. After the FIFO is reset all data outputs (DO_0 - DO_4) will be in the LOW state. As long as the FIFO remains empty the OR signal will be LOW and all Shift-Out (SO) pulses applied to it will be ignored. After data is shifted into the FIFO, the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse

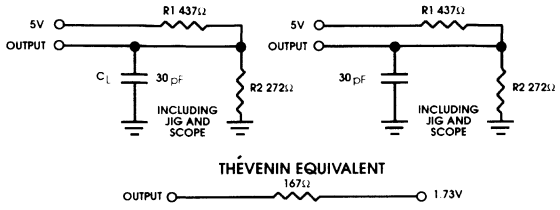
AFE AND HF FLAGS

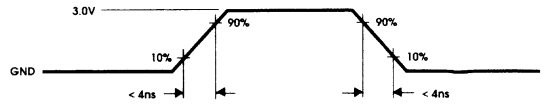
Two flags, Almost Full/Almost Empty (AFE) and Half Full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are eight or less, or 56 or more, words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO.

HF	AFE	WORDS STORED
L	H	0 - 8
L	L	9 - 31
H	L	32 - 55
H	H	56 - 64

Flag Definition Table

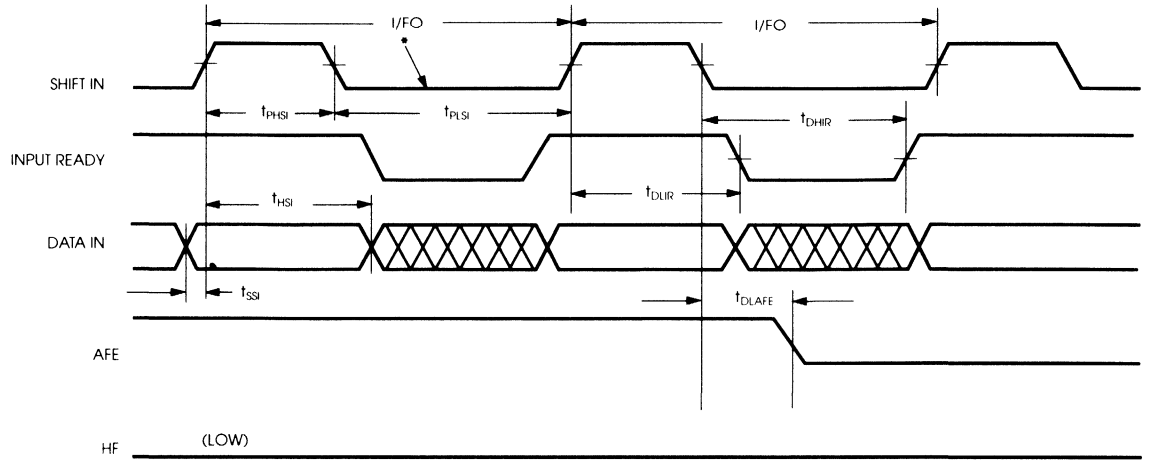
AC TEST LOAD AND WAVEFORMS



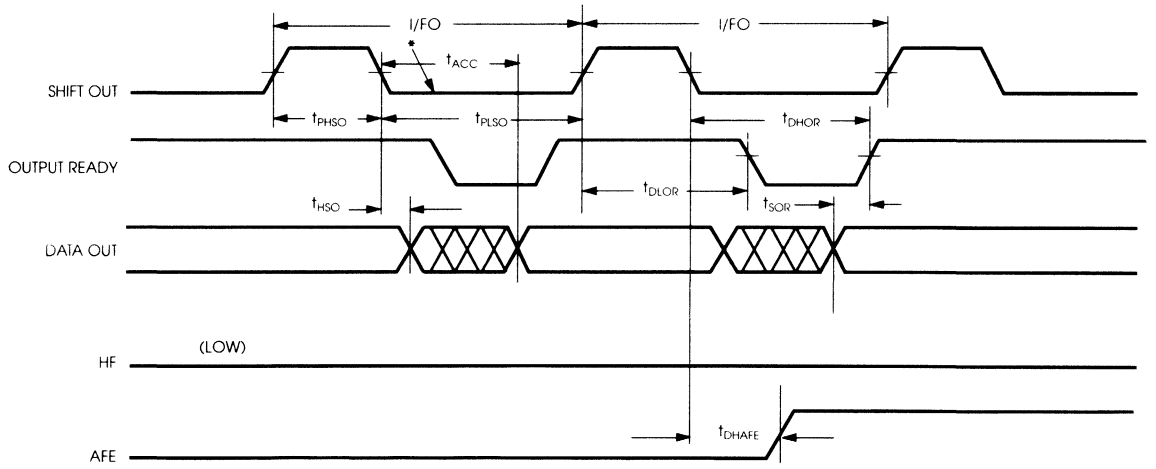


SWITCHING WAVEFORMS

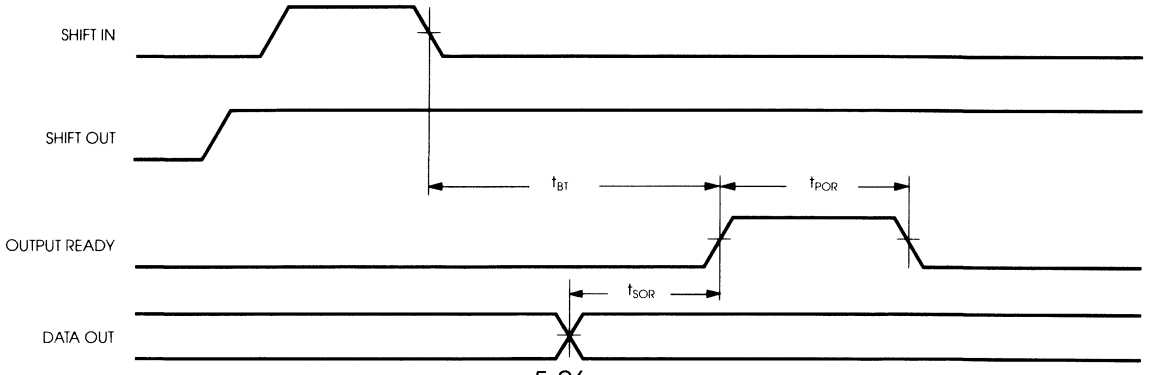
Data In Timing Diagram (FIFO Contains 8 Words)*



Data Out Timing Diagram (FIFO Contains 9 Words)*

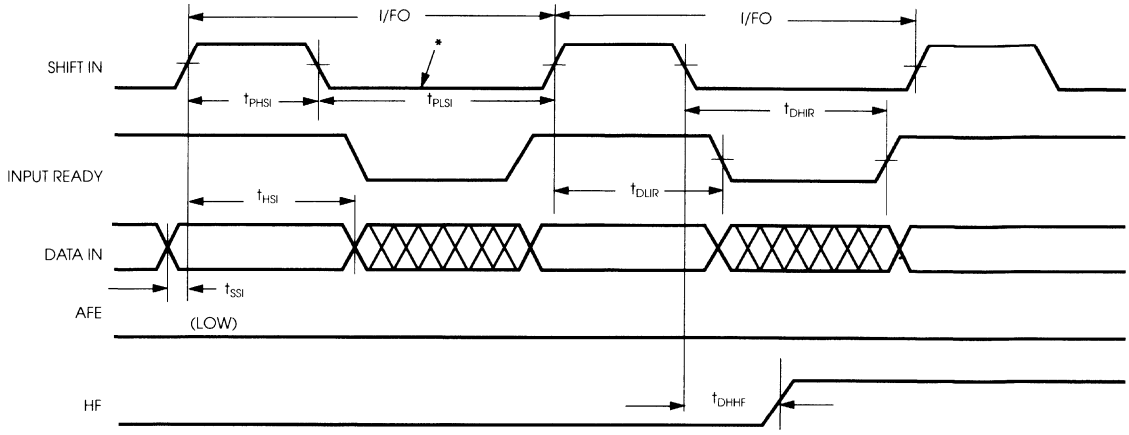


Fallthrough, (Bubblethrough) Data In to Data Out Diagram

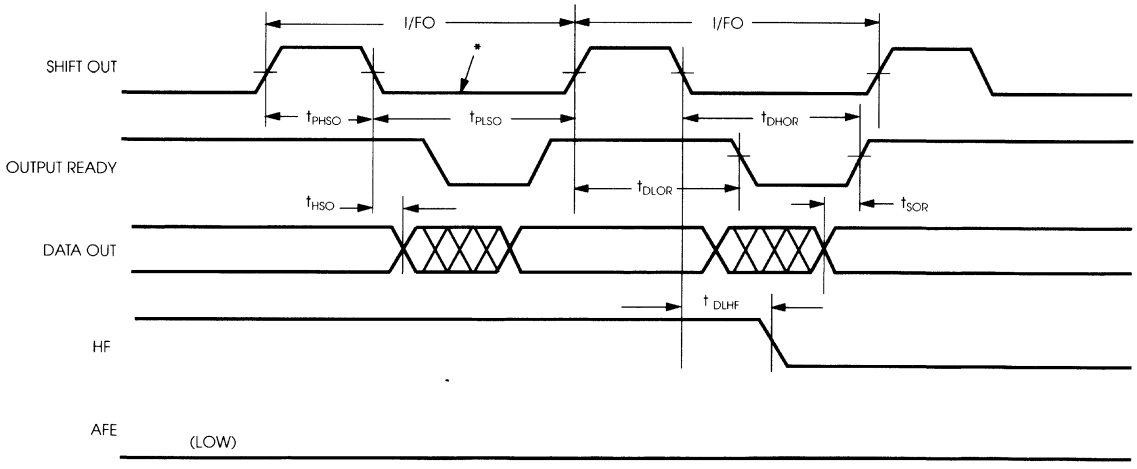


SWITCHING WAVEFORMS (CONTINUED)

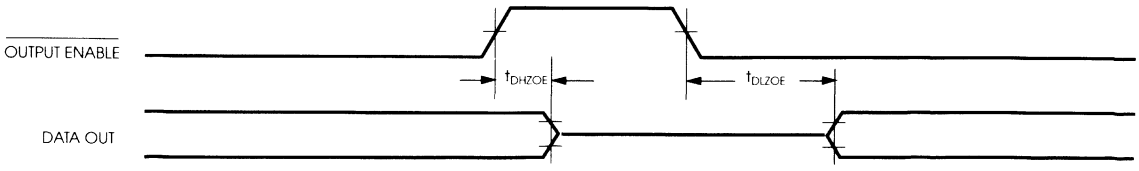
Data In Timing Diagram (FIFO Contains 31 Words)*



Data Out Timing Diagram (FIFO Contains 32 Words)*

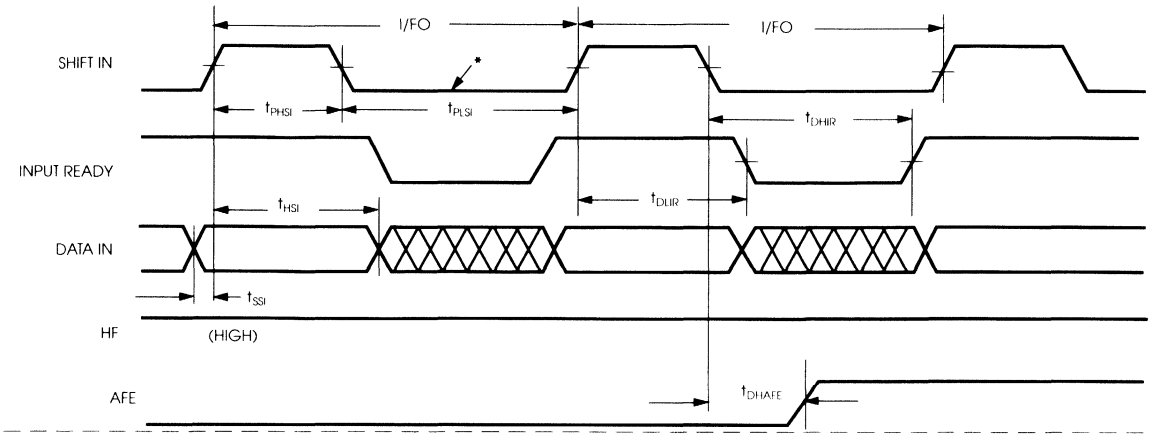


Output Enable Timing Diagram

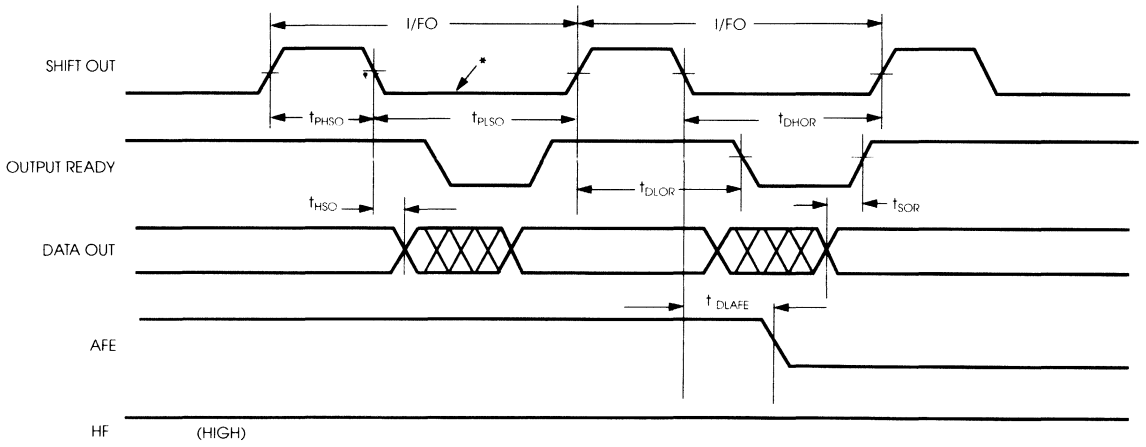


SWITCHING WAVEFORMS (CONTINUED)

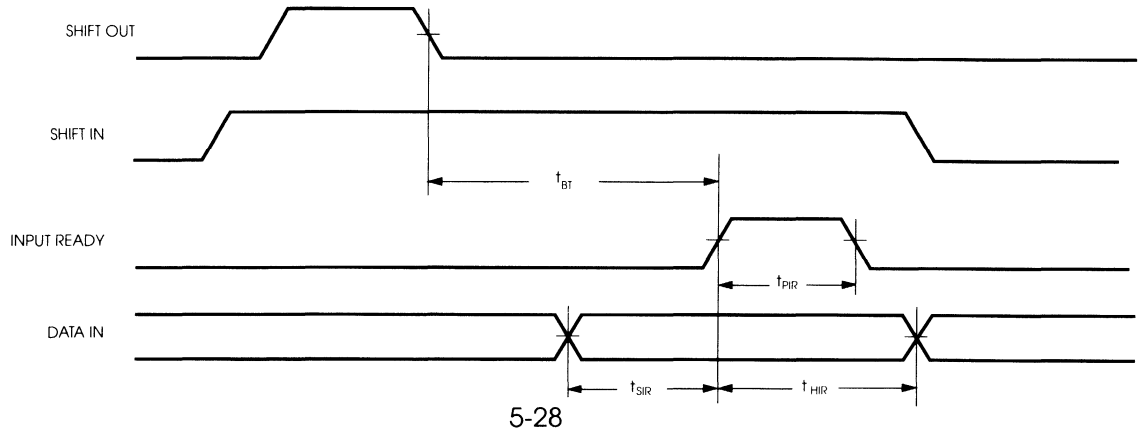
Data In Timing Diagram (FIFO Contains 55 Words)*



Data Out Timing Diagram (FIFO Contains 56 Words)*

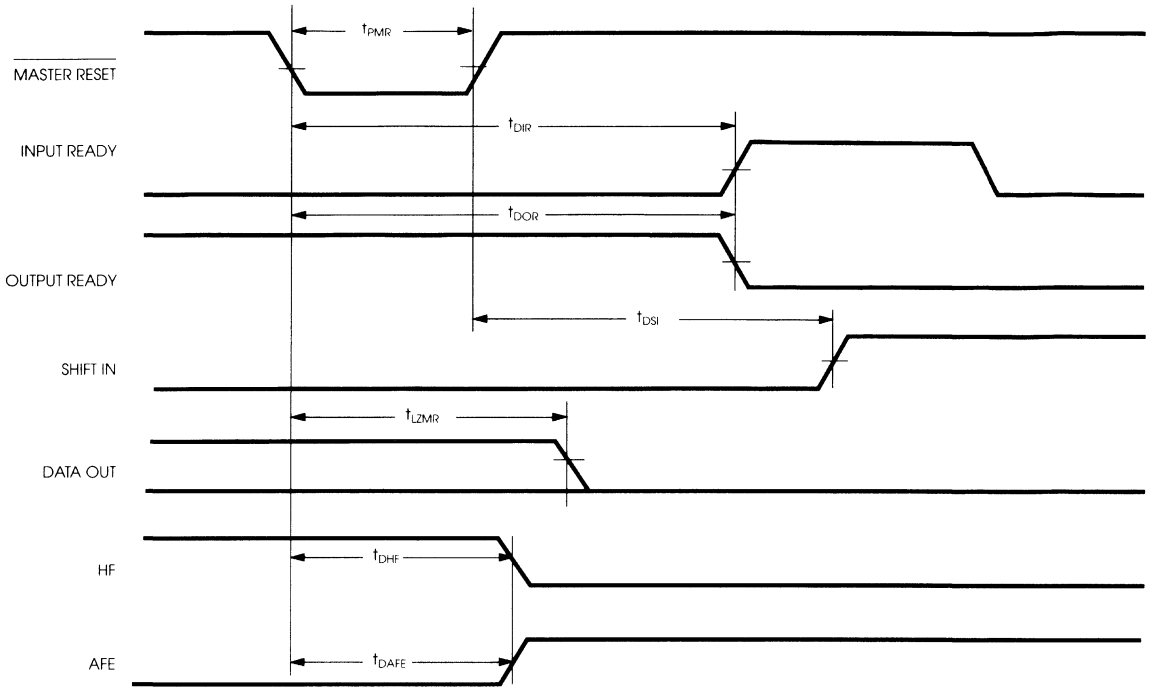


Bubblethrough, Data Out to Data In Diagram

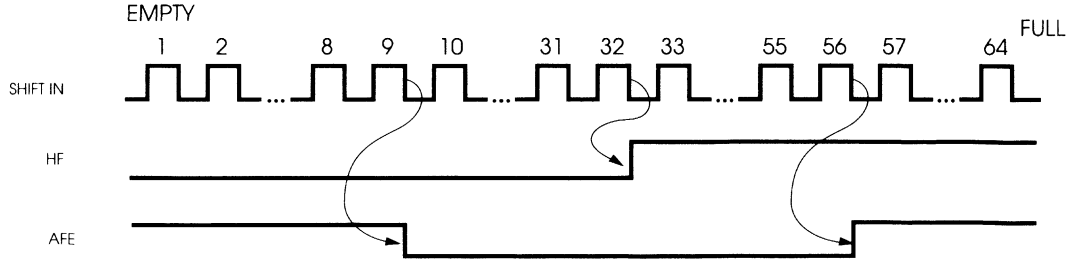


SWITCHING WAVEFORMS (CONTINUED)

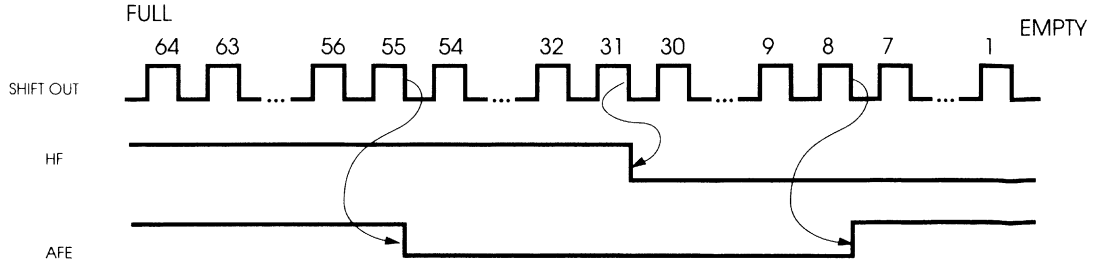
Master Reset Timing Diagram



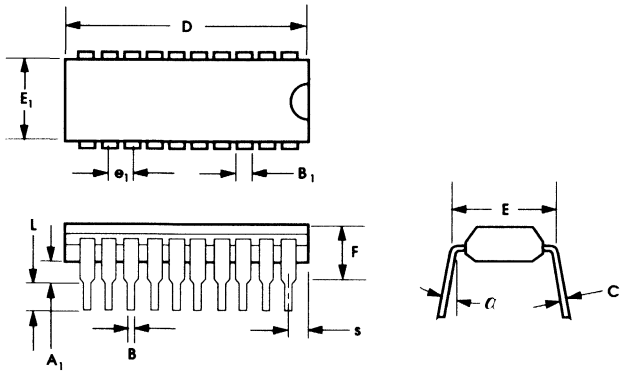
Shifting Words In



Shifting Words Out

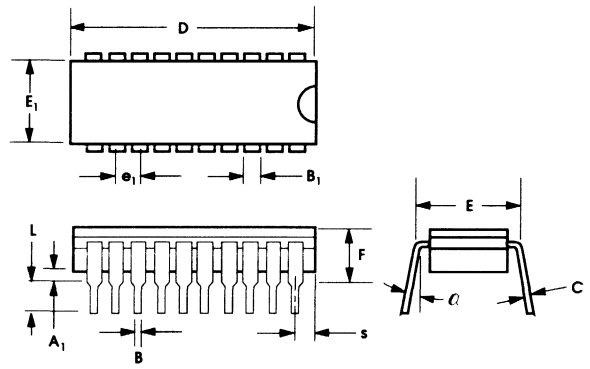


PACKAGE DIMENSIONS



20 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B_1	.045	.065
B	.016	.020
C	.008	.012
D	1.023	1.033
E	.280	.300
E_1	.245	.255
e_1	.090	.110
F		.170
L	.125	.135
s	.060	.070
α	0°	15°



20 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.060
E	.290	.320
E_1	.220	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSL7413S-50PC	50MHz	20-Pin Plastic DIP	0	+70	°C
SSL7413S-40PC	40				
SSL7413 -35PC	35				
SSL7413 -25PC	25				
SSL7413 -15PC	15				
SSL7413S-50CC	50MHz				
SSL7413S-40CC	40				
SSL7413 -35CC	35				
SSL7413 -25CC	25				
SSL7413 -15CC	15				
SSL7413S-50CM	50MHz	20-Pin CERDIP	-55	+125	°C
SSL7413S-40CM	40				
SSL7413 -35CM	35				
SSL7413 -25CM	25				
SSL7413 -15CM	15				

Saratoga Semiconductor SSL7200/1/2/3

256, 512, 1K and 2K by 9 BiCMOS TTL FIFO Buffer Memory

ADVANCE INFORMATION

FEATURES

- **Fast Acess Times**
  15/25/35/50ns max
- **Full Featured Industry Standard Devices**
  Expandable Word Widths and Depths
  Asynchronous & Simultaneous Read & Write
  Automatic Restransmit Capability
- **300 MIL and 600 MIL 28-Pin DIP Packages**
- **Full Military Temperature Range**
- **Multiple Configurations for Flexibility**
  256 X 9: 7200A, 7200B
  512 X 9: 7201, 7201A, 7201B
  1K X 9: 7202, 7202A, 7202B
  2K X 9: 7203, 7203A
  A: with HF Flag - B: with HF Flag and OE
- **SABiC BiCMOS Fabrication Technology**
  Fast Cycle Time - 30ns
  Fast Setup (5ns) & Hold (0ns) Time
  High Drive Current -16mA

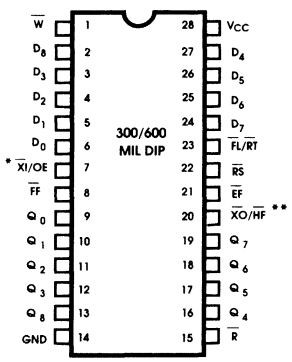
DESCRIPTION

The SSL7200, SSL7201, SSL7202 and SSL7203 are 256, 512, 1024 and 2048 words by 9-Bit wide dual port memories which function as First-In First-Out buffers. Half-Full flag is provided in the "A" version while the "B" version has both Half-Full flag and an Output Enable. These devices are fully expandable or cascadeable in word width and array depth.

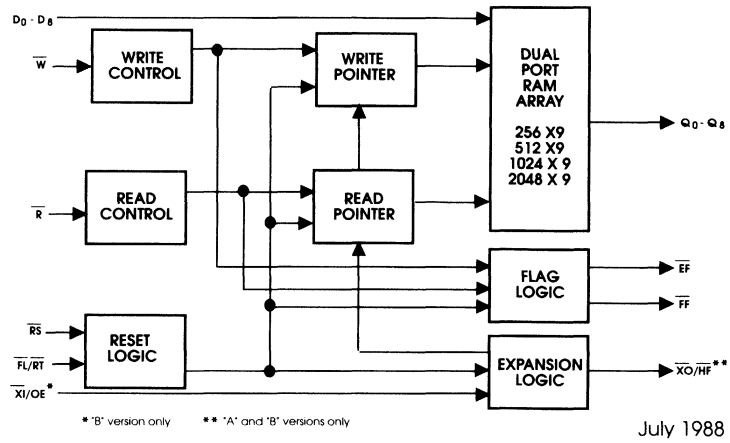
A functional block diagram is shown below. Read and write pointers are provided on the chip so that no address information is required to load or unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The read/write cycle time is as fast as 30ns or 33 MHz.

The 9-bit wide word architecture allows for parity at the user's option. This feature proves to be extremely important in data communications applications where all transmission and reception are checked for errors with the aid of the parity bit. The Retransmit ($\overline{RT}$) feature allows for resetting of the read pointer to its initial position (when $\overline{RT}$ is pulsed HIGH to LOW) where retransmission will start. A Half-full flag is available in the single device mode and width expansion modes. All four devices are available in 28-pin DIP. The SSL7203 can be obtained in a 600 MIL package, while the SSL7200, SSL7201 and SSL7202 are available in both 600 and 300 MIL form factor. (See Ordering Information on last page).

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



* "B" version only ** "A" and "B" versions only

July 1988

SELECTION GUIDE

		7200/1/2/3 -15	7200/1/2/3 -25	7200/1/2/3 -35	7200/1/2/3 -50
Maximum Shift Rate (MHz)		33.0	28.5	22.2	15.0
Maximum Operating Current (mA)	Commercial	115	110	105	95
	Military	120	115	110	100

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65 °C to + 150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in HIGH Z State	-0.5V to +7.0V
DC Input Voltage	-0.8V to +7.0V
Power Dissipation	1.0W
Output Current, into Outputs (Low)	20mA
Static Discharge Voltage (per MIL-STD 883 Method 3015.2)	>2001V
Latch-Up Current	>200mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0 °C to +70 °C	5V ± 10%
Military	-55 °C to +125 °C	5V ± 10%

ELECTRICAL CHARACTERISTICS (Over Operating Range, unless Otherwise Noted)

PARAMETERS	DESCRIPTION	TEST CONDITIONS		SSL7200/1/2/3 15, 25, 35, 50 MIN	SSL7200/1/2/3 15, 25, 35, 50 MAX	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			-0.5	0.8	V
I_{IX}	Input Leakage Current (1)	GND ≤ V_I ≤ V_{CC}, V_{CC} = max		-10	+10	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = GND			-150	mA
I_{OZ}	Output Leakage Current (2)	OE = V_{IH}, V_{CC} = max GND≤ V_{OUT} ≤ V_{CC}		-50	50	mA
I_{CC1}	Operating Current (3)	V_{CC} = Max, I_{OUT} = 0mA;	Commercial		100	mA
			Military		120	mA
I_{CC2}	Standby Current (3)	$\overline{R}$ = $\overline{W}$ = $\overline{MR}$ = FL/$\overline{RT}$ = V_{IH}	Commercial		90	mA
			Military		95	mA
I_{CC3}	Power Down Current (3)	All Inputs Vcc - 0.2V	Commercial		TBD	mA
			Military		TBD	mA

CAPACITANCE (4)

PARAMETERS	DESCRIPTION	TEST CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC}= 4.5V	7	pF

Notes: [1] Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}
[2] $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}
[3] I_{CC} measurements are made with outputs open.
[4] This parameter is sampled and not 100% tested.

SWITCHING CHARACTERISTICS Over the Operating Range

PARAMETER	DESCRIPTION	TEST CONDITIONS	SSL720X -15		SSL720X -25		SSL720X -35		SSL720X -50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_S	Shift Frequency-Com/MIL			33.0		28.5		22.2		15.0	MHz
t_{RC}	Read Cycle Time	Note 6	30		35/40		45		65		ns
t_{A1}	Access Time			15		25		35		50	ns
t_{RR}	Read Recovery Time	Note 6	15/20		15/20		15/20		20		ns
t_{RPW}	Read Pulse Width	Note 2	15		20		30		50		ns
t_{RLZ}	Read Pulse LOW to Bus at LOW Z	Note 3	5		5		5		5		ns
t_{WLZ}	Write Pulse LOW to Bus at LOW Z	Note 3,4	10		10		10		10		ns
t_{DV}	Data Valid from Read Pulse HIGH		5		5		5		5		ns
t_{RHZ}	Read Pulse HIGH to Bus at HIGH Z	Note 3, 6		18		18/23		20/25		30	ns
t_{WC}	Write Cycle Time	Note 6	30		35/40		45		65		ns
t_{WPW}	Write Pulse Width	Note 2	15		20		30		50		ns
t_{WR}	Write Recovery Time	Note 6	15/20		15/20		15/20		15/20		ns
t_{DS}	Data Set-Up Time		8		15		18		30		ns
t_{DH}	Data Hold Time	Note 6	0		0/1		0/1		0/1		ns
t_{RSC}	Reset Cycle Time		25		35		45		65		ns
t_{RS}	Reset Pulse Width	Note 2	10		25		35		50		ns
t_{RSR}	Reset Recovery Time		5		10		10		15		ns
t_{RTC}	Retransmit Cycle time		25		35		45		65		ns
t_{RT}	Retransmit Pulse Width	Note 2	15		25		35		50		ns
t_{RTR}	Retransmit Recovery Time		10		10		10		15		ns
t_{EFL}	Reset to Empty Flag LOW	Note 6		35		35/40		45		65	ns
$t_{HFH/FFH}$	Reset to Half-Full and Full Flag HIGH	Note 6		35		35/40		45		65	ns
t_{REF}	Read LOW to Empty Flag LOW	Note 6		25		25/30		30		45	ns
t_{RFF}	Read HIGH to Full Flag HIGH	Note 6		25		25/30		30		45	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	Note 6		25		25/30		30		45	ns
t_{WFF}	Write LOW to Full Flag LOW	Note 6		25		25/30		30		45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	Note 6		25		35/40		45		65	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	Note 6		25		35/40		45		65	ns
t_{OES}	OE HIGH to $\overline{R}$ HIGH Set-Up Time	Note 7									ns
t_{OER}	OE LOW to $\overline{R}$ HIGH Recovery Time	Note 7									ns
t_{A2}	Data Access Time from $\overline{R}$ HIGH	Note 7									ns
t_{RHZ}	$\overline{R}$ HIGH to Data Output HIGH Z	Note 7									ns
t_{ROES}	$\overline{R}$ to OE Set-Up Time	Note 7									ns
t_{ROER}	OE to $\overline{R}$ Recovery Time	Note 7									ns
t_{LZOE}	OE HIGH to Output Enable	Note 7									ns
t_{HZOE}	OE LOW to Output HIGH Z	Note 7									ns

NOTES:
1 Timings referenced as in AC Test Conditions.
2 Pulse width less than minimum value are not allowed.
3 Values guaranteed by design, not currently tested.
4 Only applies to read data flow through mode.
5 Generating R and W signals: When using these high speed FIFO devices, it is necessary to have clean inputs on the R and W signals. It is important to be glitch free, spikes free and free of ringing with respect to V_{IL} and V_{IH} requirements. A glitch of only a few nanoseconds on the $\overline{R}$ and $\overline{W}$ pulses may cause improper operation in the read and write pointers.
6 Two values in a given column represent first the Commercial and then the Military Temperature specifications.
7 "B" version only.

OPERATING DESCRIPTION

INPUTS

DATA IN (D_0 - D_8): Data inputs for 9-bit wide data bus.

RESET ($\overline{RS}$): Reset ($\overline{RS}$) is low active. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in a HIGH state during the window shown in the Reset Timing Diagram (next page), ie, T_{RPW} or T_{WPW} before the rising edge of RS, and should not change until T_{RSR} after the rising edge of RS. Half-Full Flag ($\overline{HF}$) will be reset to HIGH after master Reset (RS).

WRITE ENABLE ($\overline{W}$): A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointers is less than or equal to one half of the total memory size of that device. The Half-Full Flag is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW , inhibiting further write operations. Upon completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after T_{RFF} , allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from ($\overline{W}$), so external changes in ($\overline{W}$) will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$): A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a Firsst-In First-Out basis, independent of any on-going write operations.

After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (D_0 - D_8) will return to a HIGH impedance state until the next read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the"final" read cycle but inhibiting further read operations with the data outputs remaining in a HIGH impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after T_{WEF} , and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from ($\overline{R}$), so external changes in ($\overline{R}$) will not affect the FIFO when it is empty.

FIRST LOAD/RESTRANSMIT ($\overline{FL}/\overline{RT}$): This is a dual purpose input. For depth expansion, the pin is grounded to indicate it is the first load. (See Operating Modes). In the single device mode, this pin acts as the retransmit input. The single device mode is initiated by grounding the EXPANSION IN ($\overline{XI}$) pin.

These devices can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable (R) and Write Enable (W) must be in the HIGH state during retransmit. This feature is useful when less than the full (256, 512, 1024 or 2048 words respectively) number of writes are performed between resets. The retransmit feature is not compatible with depth expansion mode, and will affect the Half-Full Flag ($\overline{HF}$) depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$): This input is a dual purpose pin. EXPANSION IN ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In is connected to Expansion Out ($\overline{XO}$) of the previous device for depth expnasion or daisy chain mode.

OUTPUTS

FULL FLAG ($\overline{FF}$): The Full Flag will go LOW inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after Reset, the Full Flag will go LOW after 256, 512, 1024 or 2048 writes respectively, for the SSL7200, SSL7201, SSL7202 or SSL7203.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$): This is a dual purpose output. In the single mode, when Expansion IN ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Falg ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion mode, Expansion IN ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the daisy chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0 - Q_8): Data output for the 9-bit wide data bus. When ($\overline{R}$) is HIGH, this bus will be in a high impedance state.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise & Fall Times	4ns
Input Reference Level	1.5V
Output Reference Level	1.5V
Output Load	See Figure 1

* Includes jig and scope capacitances.

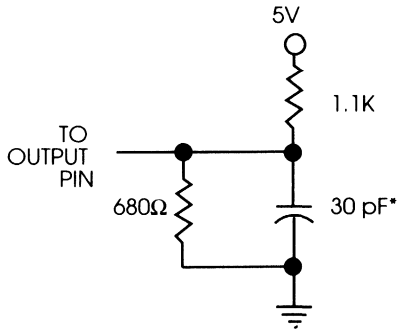
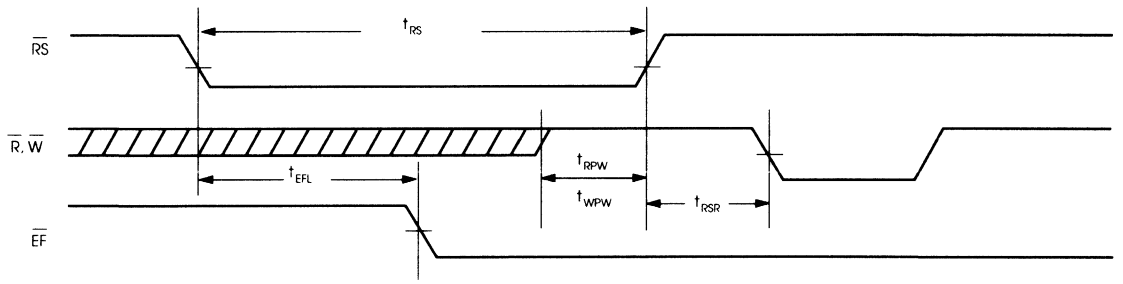


Figure 1. OUTPUT LOAD

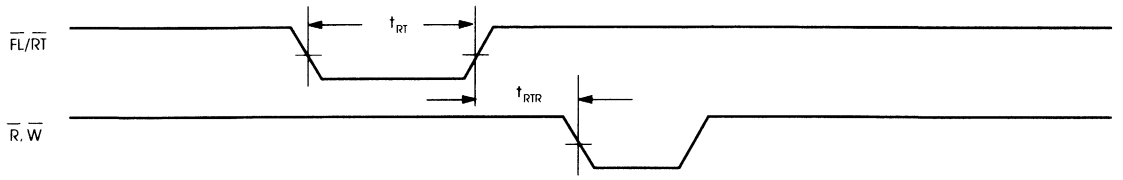
SWITCHING WAVEFORMS

Reset Timing



NOTE: $t_{RSC} = t_{RS} + t_{RSR}$

Retransmit Timing

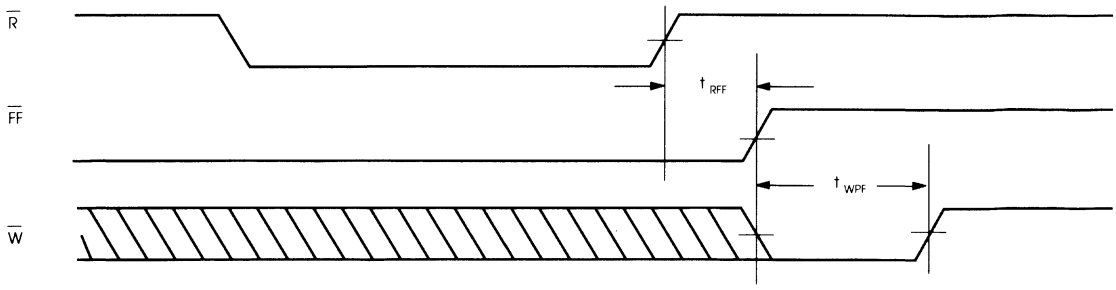


NOTE: $t_{RTC} = t_{RT} + t_{RTR}$

SWITCHING WAVEFORMS (CONTINUED)

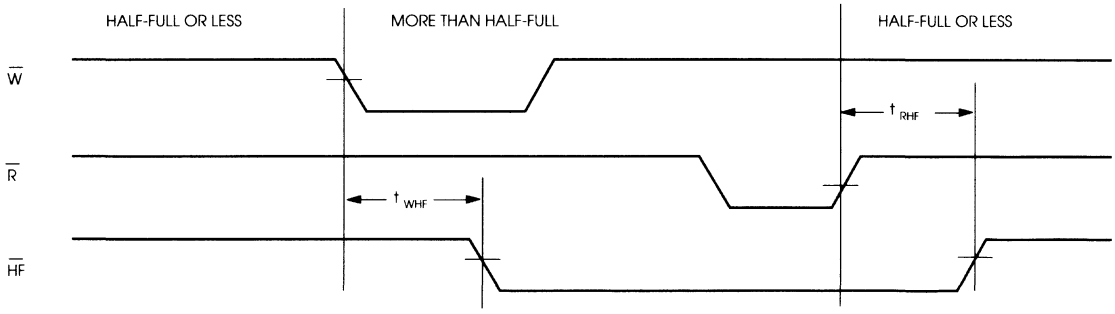
Full Flag Timing

t_{WPF}= Effective Write Pulse Width After Full Flag HIGH.



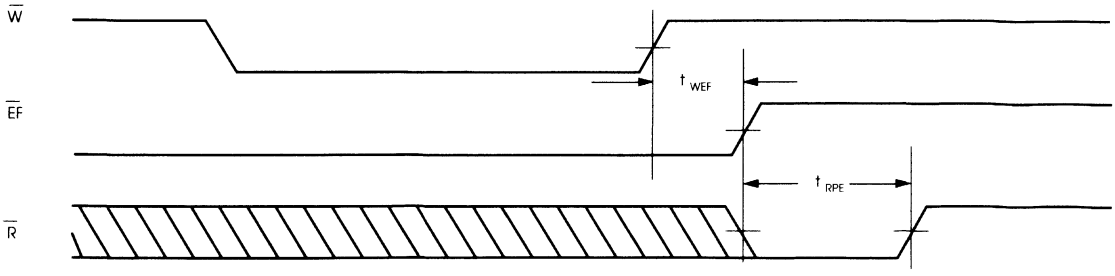
NOTE: $t_{WPF} = t_{WPW}$.

Half-Full Flag Timing



Empty Flag Timing

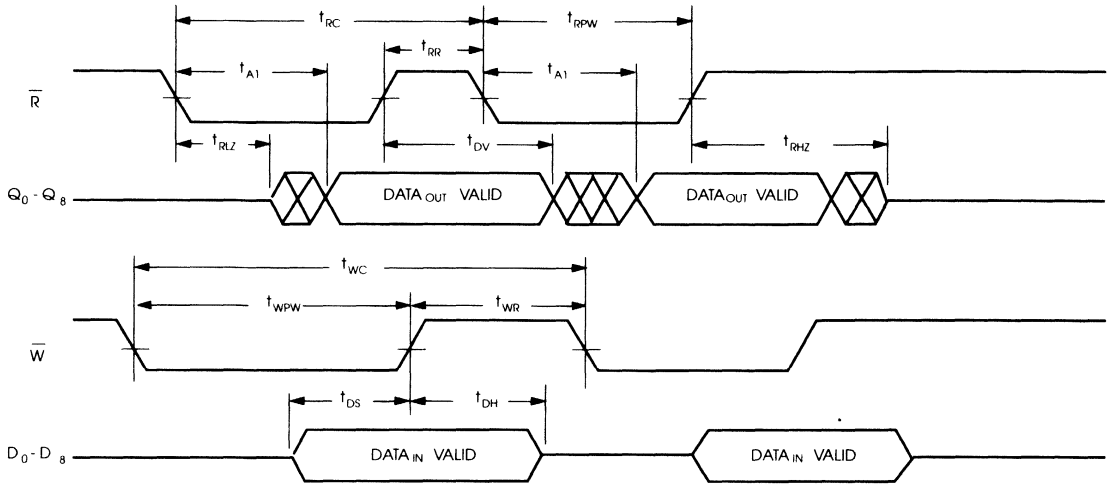
t_{RPE} = Effective Read Pulse Width After Empty Flag HIGH.



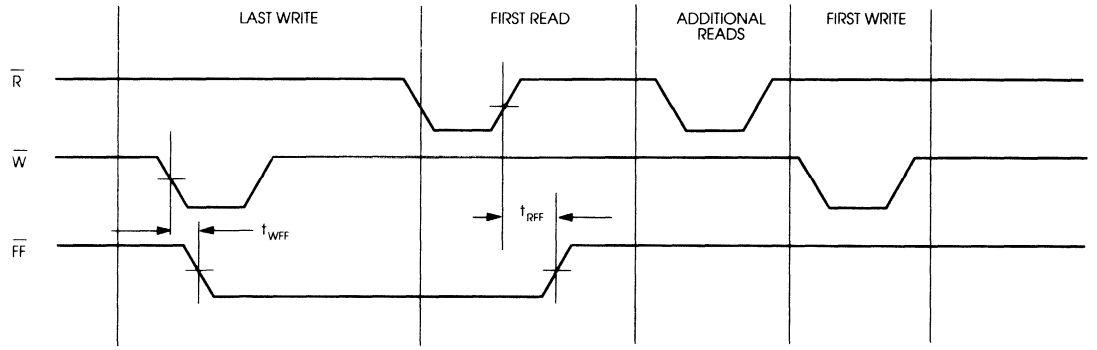
NOTE: $t_{RPE} = t_{RPW}$.

SWITCHING WAVEFORMS (CONTINUED)

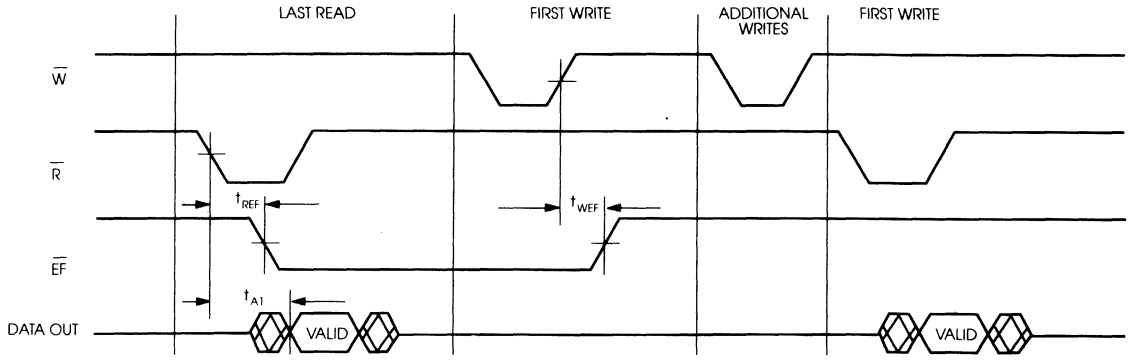
Asynchronous Write and Read Operation



Full Flag from Last Write to First Read



Empty Flag from Last Read to First Write



OUTPUT ENABLE FUNCTIONALITY ("B" VERSION)

Initial state is determined by the state of the $\overline{FL}/\overline{RT}$ and $\overline{XI}/OE$ pins during rising edge of the $\overline{RS}$ signal.

After RESET to the CASCADE mode, the $\overline{FL}/\overline{RT}$ pin should be held constant. The $\overline{XI}/OE$ pin accepts pulses to enable the READ or WRITE clocks respectively for proper cascading. The $\overline{XO}/\overline{HF}$ pin generates the $\overline{XI}$ pulse to be used by the next device in the cascade daisy chain.

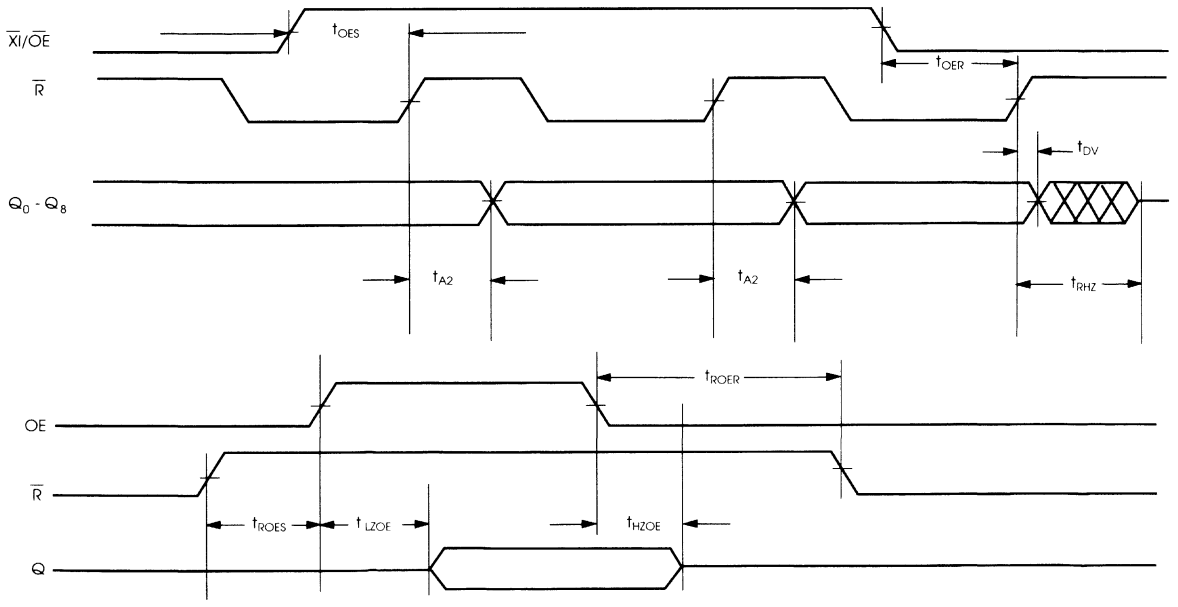
Aafter RESET to the STANDALONE mode, the $\overline{FL}/\overline{RT}$ acts as a retransmit control for the FIFO. Retransmit resets the READ pointer to the Zero location without effecting the WRITE pointer. The $\overline{FF}$, $\overline{EF}$ and $\overline{XO}/\overline{HF}$ Flags are adjusted accordingly. The $\overline{XO}/\overline{HF}$ output acts as a Half Full Flag in this mode of operation. The control of the Outputs follows this table in the STANDALONE mode.

STATE	$\overline{XI}/OE$	$\overline{FL}/\overline{RT}$
STANDALONE	0	0
STANDALONE	0	1
CASCADE FIRST LOAD	1	0
CASCADE DISABLED	1	1

DESCRIPTION / MODE	COMMENT	OUTPUTS "A" VERSION	OUTPUTS "B" VERSION	$\overline{XI}/OE$	$\overline{R}$
1	MEMORY LIKE OUTPUT	ENABLED	ENABLED	0	0
		HIGH-Z	HIGH-Z	0	1
2	REGISTER LIKE OUTPUT	ENABLED	ENABLED	1	0
		HIGH-Z	ENABLED	1	1

In mode 1, version "B" acts exactly as version "A". In mode 2, version "B" outputs act like Register outputs instead of Memory outputs, i.e. Output data change from valid data to valid data on the upgoing edge of READ ($\overline{R}$) instead of from valid data through HIGH Z to next valid data on the down going edge of READ ($\overline{R}$).

SWITCHING WAVEFORMS ("B" VERSION)



OPERATING MODES

SINGLE DEVICE MODE

The SSL7200/1/2/3 can be used in single device mode. To do so, simply ground the Expansion In (XI) control input pin as shown in Figure 2. In this mode the Half-Full Flag ($\overline{HF}$), which is an active LOW output, is shared with Expansion Out (XO).

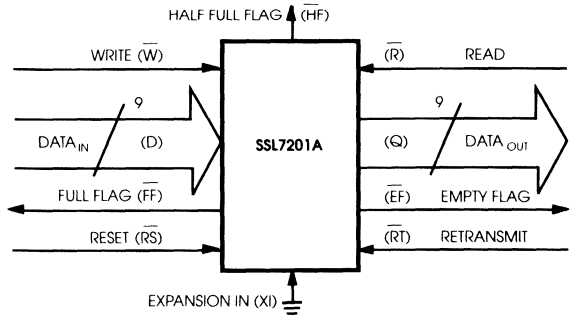


Figure 2. BLOCK DIAGRAM OF SINGLE 512 X 9 FIFO.

WIDTH EXPANSION MODE

Word width may be increased by connecting the corresponding input control signals of multiple devices. Status flags (EF, FF and HF) can be detected from any one device. Figure 3 is an example of an 18-bit word width by using two devices of the same density. Wider word width can thus be accomplished by adding more devices in the same fashion.

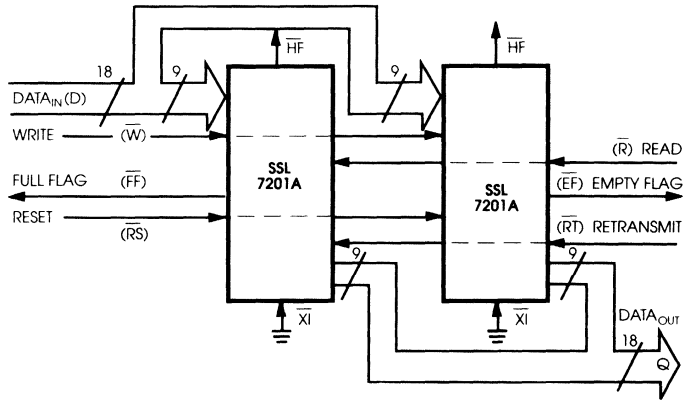


Figure 3. BLOCK DIAGRAM OF 512 X 18 FIFO MEMORY USED IN WIDTH EXPANSION MODE

DEPTH EXPANSION (Daisy Chain) MODE

If an application requires more words than a particula chosen device can provide, depth expansion is possible by connecting multiple devices of the same kind as shown in Figure 4. When the expansion mode is used, be sure the following conditions are met:

1) The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2) All other devices must have (FL) in the HIGH state.
3) The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device as shown in Figure 4.
4) External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the "ORing" of all $\overline{EF}$s and "ORing" of all $\overline{FF}$s.
5) The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the depth expansion mode.

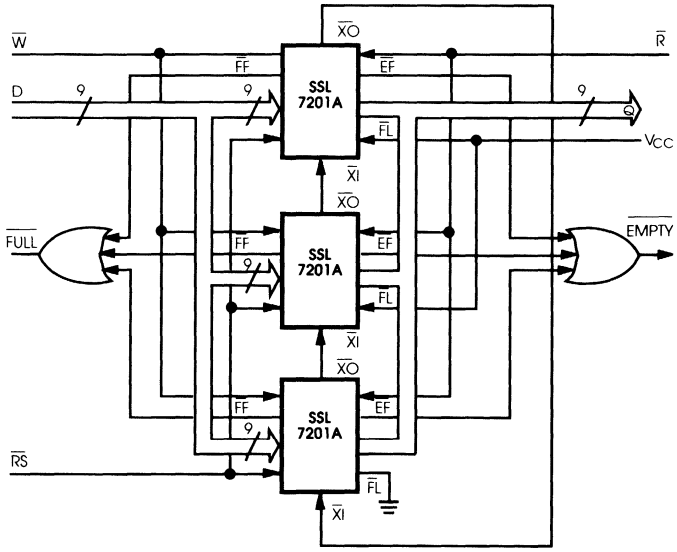


Figure 4. BLOCK DIAGRAM OF 1536 X 9 FIFO MEMORY (DEPTH EXPANSION)

OPERATING MODES (CONTINUED)

COMPOUND EXPANSION MODE

The two methods described above can be applied together to achieve large FIFO arrays. See Figure 5.

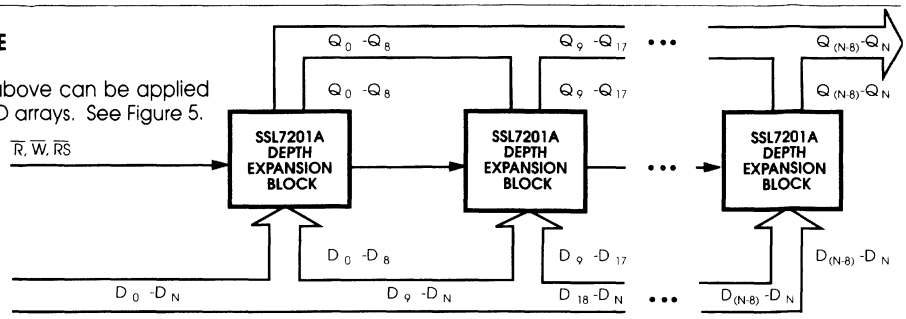


Figure 5. COMPOUND FIFO EXPANSION.

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of read and write operations) can be achieved by pairing the FIFO devices as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system; i.e. ($\overline{FF}$) is monitored on the device where ($\overline{W}$) is used and ($\overline{EF}$) is monitored on the device where ($\overline{R}$) is used. Both depth and width expansion may be used in this mode.

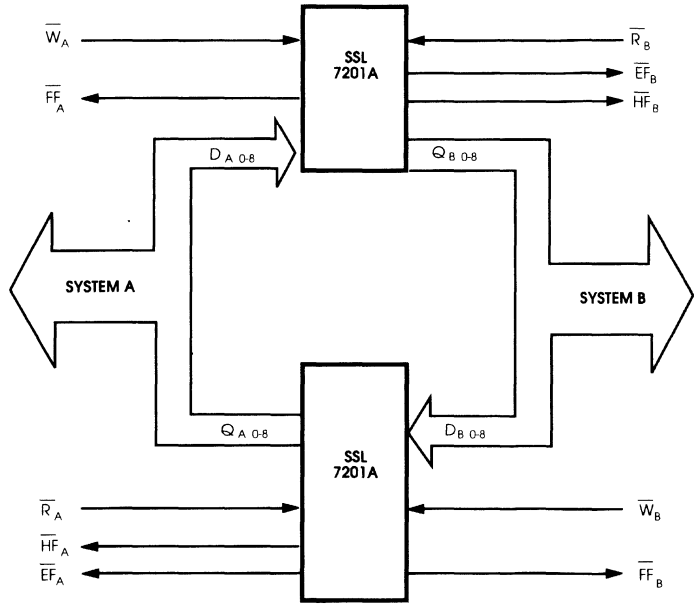


Figure 6. BIDIRECTIONAL FIFO MODE.

TABLE I. RESET AND TRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Location Zero	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

Notes:

(1) Pointer will increment if Flag is HIGH.

OPERATING MODES (CONTINUED)

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted, a read flow-through and a write flow-through. For the read flow-through (Figure 7), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (T_{WEF} +T_A) ns after the rising edge of ($\overline{W}$), called the first write edge, and it remains on the bus until the ($\overline{R}$) line is raised from LOW to HIGH, after which the bus would go into a three-state mode after T_{RHZ} ns. The ($\overline{EF}$) line would have a pulse showing temporary de-assertion and then would be asserted. During the time when ($\overline{R}$) is LOW, more words can be written to the FIFO (the subsequent writes after the first write edge would de-assert the empty flag), however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when ($\overline{R}$) is LOW. On toggling ($\overline{R}$), the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through (Figure 8), the FIFO permits the writing edge of a single word of data immediately after reading one word of data from a full FIFO. The ($\overline{R}$) line causes the FF to be de-asserted, but the ($\overline{W}$) line being LOW causes the FIFO to be asserted again in anticipation of a data word. On the rising edge of ($\overline{W}$), the new word is loaded into the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

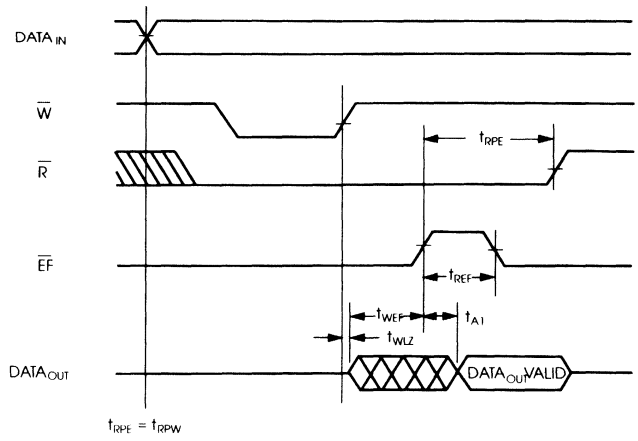


Figure 7. READ DATA FLOW-THROUGH MODE

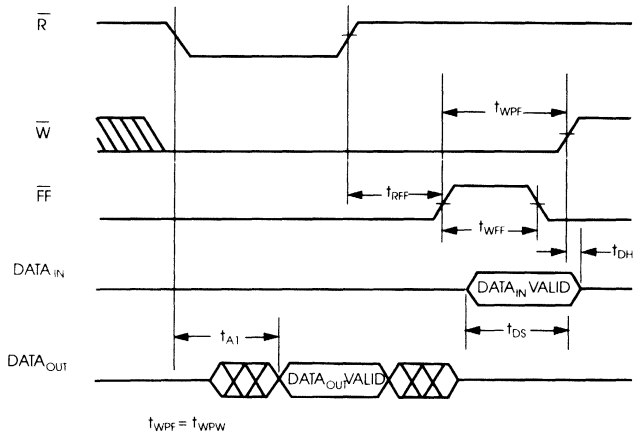


Figure 8. WRITE DATA FLOW-THROUGH MODE

TABLE II. RESET AND FIRST LOAD TRUTH TABLE

DEPTH EXPANSION/COMPOUND EXPANSION MODE

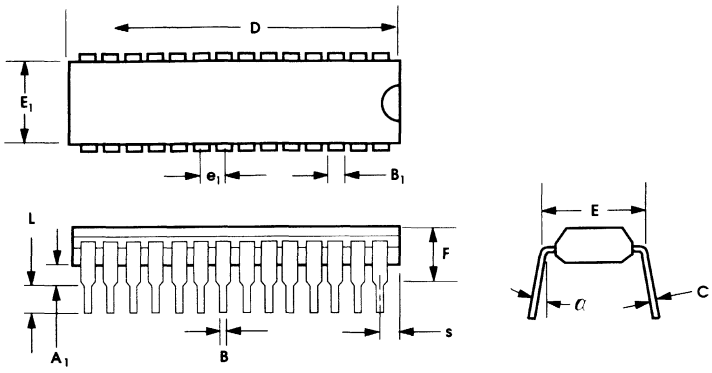
MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Notes:

[1] $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 4.

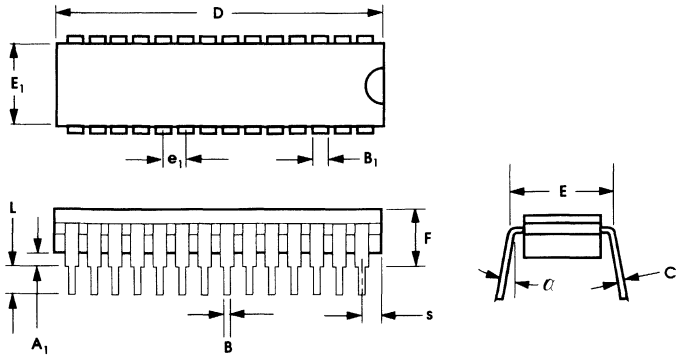
$\overline{RS}$ = Reset input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

PACKAGE DIMENSIONS



28 LEAD 300/600 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES			
	300 MIL		600 MIL	
PARAMETER	MIN	MAX	MIN	MAX
A_1	.015		.015	
B	.016	.020	.016	.020
B_1	.045	.055	.055	.065
C	.008	.012	.008	.012
D	1.345	1.355	1.445	1.455
E	.300	.325	.600	.625
E_1	.270	.290	.530	.550
e_1	.090	.110	.090	.110
F		.170		.190
L	.125	.135	.125	.135
s	.020	.030	.070	.080
α	0°	15°	0°	15°



28 LEAD 600 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.490
E	.590	.620
E_1	.500	.610
e_1	.090	.110
F		.232
L	.125	.200
s		.100
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSL7200A-15PC3	15ns	28-Pin 300 MIL Plastic DIP	0	+70	°C
SSL7200A-25PC3	25				
SSL7200A-35PC3	35				
SSL7200A-50PC3	50				
SSL7200B-15PC3	15ns				
SSL7200B-25PC3	25				
SSL7200B-35PC3	35				
SSL7200B-50PC3	50				
SSL7201-15PC3	15ns	28-Pin 300 MIL Plastic DIP			
SSL7201-25PC3	25				
SSL7201-35PC3	35				
SSL7201-50PC3	50				
SSL7201A-15PC3	15ns				
SSL7201A-25PC3	25				
SSL7201A-35PC3	35				
SSL7201A-50PC3	50				
SSL7201B-15PC3	15ns				
SSL7201B-25PC3	25				
SSL7201B-35PC3	35				
SSL7201B-50PC3	50				
SSL7202-15PC3	15ns	28-Pin 300 MIL Plastic DIP			
SSL7202-25PC3	25				
SSL7202-35PC3	35				
SSL7202-50PC3	50				
SSL7202A-15PC3	15ns				
SSL7202A-25PC3	25				
SSL7202A-35PC3	35				
SSL7202A-50PC3	50				
SSL7202B-15PC3	15ns				
SSL7202B-25PC3	25				
SSL7202B-35PC3	35				
SSL7202B-50PC3	50				
SSL7200A-15PC	15ns	28-Pin 600 MIL Plastic DIP			
SSL7200A-25PC	25				
SSL7200A-35PC	35				
SSL7200A-50PC	50				
SSL7200B-15PC	15ns				
SSL7200B-25PC	25				
SSL7200B-35PC	35				
SSL7200B-50PC	50				
SSL7201-15PC	15ns	28-Pin 600 MIL Plastic DIP			
SSL7201-25PC	25				
SSL7201-35PC	35				
SSL7201-50PC	50				
SSL7201A-15PC	15ns				
SSL7201A-25PC	25				
SSL7201A-35PC	35				
SSL7201A-50PC	50				
SSL7201B-15PC	15ns				
SSL7201B-25PC	25				
SSL7201B-35PC	35				
SSL7201B-50PC	50				

ORDERING INFORMATION (CONTINUED)

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSL7202-15PC	15ns	28-Pin 600 MIL Plastic DIP	0	+70	°C
SSL7202-25PC	25				
SSL7202-35PC	35				
SSL7202-50PC	50				
SSL7202A-15PC	15ns				
SSL7202A-25PC	25				
SSL7202A-35PC	35				
SSL7202A-50PC	50				
SSL7202B-15PC	15ns				
SSL7202B-25PC	25				
SSL7202B-35PC	35				
SSL7202B-50PC	50				
SSL7203-15PC	15ns	28-Pin 600 MIL Plastic DIP			
SSL7203-25PC	25				
SSL7203-35PC	35				
SSL7203-50PC	50				
SSL7203A-15PC	15ns				
SSL7203A-25PC	25				
SSL7203A-35PC	35				
SSL7203A-50PC	50				
SSL7200A-15CC	15ns	28-Pin 600 MIL CERDIP			
SSL7200A-25CC	25				
SSL7200A-35CC	35				
SSL7200A-50CC	50				
SSL7200B-15CC	15ns				
SSL7200B-25CC	25				
SSL7200B-35CC	35				
SSL7200B-50CC	50				
SSL7201-15CC	15ns	28-Pin 600 MIL CERDIP			
SSL7201-25CC	25				
SSL7201-35CC	35				
SSL7201-50CC	50				
SSL7201A-15CC	15ns				
SSL7201A-25CC	25				
SSL7201A-35CC	35				
SSL7201A-50CC	50				
SSL7201B-15CC	15ns				
SSL7201B-25CC	25				
SSL7201B-35CC	35				
SSL7201B-50CC	50				
SSL7202-15CC	15ns	28-Pin 600 MIL CERDIP			
SSL7202-25CC	25				
SSL7202-35CC	35				
SSL7202-50CC	50				
SSL7202A-15CC	15ns				
SSL7202A-25CC	25				
SSL7202A-35CC	35				
SSL7202A-50CC	50				
SSL7202B-15CC	15ns				
SSL7202B-25CC	25				
SSL7202B-35CC	35				
SSL7202B-50CC	50				
SSL7203-15CC	15ns	28-Pin 600 MIL CERDIP			
SSL7203-25CC	25				
SSL7203-35CC	35				
SSL7203-50CC	50				
SSL7203A-15CC	15ns				
SSL7203A-25CC	25				
SSL7203A-35CC	35				
SSL7203A-50CC	50				

ORDERING INFORMATION (CONTINUED)

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSL7200A-25CM	25ns	28-Pin 600 MIL CERDIP	-55	+125	°C
SSL7200A-35CM	35				
SSL7200A-50CM	50				
SSL7200B-25CM	25ns				
SSL7200B-35CM	35				
SSL7200B-50CM	50				
SSL7201-25CM	25ns	28-Pin 600 MIL CERDIP			
SSL7201-35CM	35				
SSL7201-50CM	50				
SSL7201A-25CM	25ns				
SSL7201A-35CM	35				
SSL7201A-50CM	50				
SSL7201B-25CM	25ns				
SSL7201B-35CM	35				
SSL7201B-50CM	50				
SSL7202-25CM	25ns	28-Pin 600 MIL CERDIP			
SSL7202-35CM	35				
SSL7202-50CM	50				
SSL7202A-25CM	25ns				
SSL7202A-35CM	35				
SSL7202A-50CM	50				
SSL7202B-25CM	25ns				
SSL7202B-35CM	35				
SSL7202B-50CM	50				
SSL7203A-25CM	25ns	28-Pin 600 MIL CERDIP			
SSL7203A-35CM	35				
SSL7203A-50CM	50				
SSL7203B-25CM	25ns				
SSL7203B-35CM	35				
SSL7203B-50CM	50				

Saratoga Semiconductor **SSL72432/4/5/6**

128 Words by 18, 32 and 36 Bit BiCMOS Bi-Directional FIFO

PRELIMINARY INFORMATION

FEATURES

- **Family of Wide-Bus, Bi-Directional FIFOs**
  SSL72436: 128 Words by 36 Bits Array (36-bit Port P and 36-bit Port Q)
  SSL72432: 128 Words by 32 Bits Array (32-bit Port P and 32-bit Port Q)
  SSL72434: 128 Words by 18 Bits Array (18-bit Port P and 18-bit Port Q)
  SSL72435: 128 Words by 36 Bits Array (18-bit Port P and 36-bit Port Q)

- **High Speed Operations**
  Port Q Data Access = 10ns max
  Port P Data Access = 12.5ns max
  Port P Byte Access = 10ns max
  Fast Setup (5ns) & Hold (0ns max) Time

- **Full Military Temperature Range**

- **Functional Flags per Part Type**
  SSL72436: Full, Empty, Half-Full, Almost Full/Empty, and Parity Error Flags for each Port
  SSL72432: Full, Empty and Half-Full for each Port
  SSL72434: Full, Empty and Half-Full for each Port
  SSL72435: Full, Empty, Almost Full/Empty, and Half Full for each Port

- **Full Featured for Design Flexibility**
  Port to Port Flow Through Mode
  Request & Aknowledge Pins for SSL72436
  Programmable HF and AFE Flags during Reset
  Programmable Read and Write Break Points

- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

This Family of Bi-Directional FIFOs consists of four members, the SSL72436, SSL72432, SSL72434 and SSL72435. A functional blockdiagram of each device type is shown in Figures 1, 2, 3 and 4 respectively. All FIFOs in this family have Bi-Directional buses as part of their architectural features.

The SSL72436 is a dual-ported, 128 x 36 FIFO with two 36-bit Bi-Directional buses (Port P and Port Q). Byte handling capability is provided on Port P, where selection of random byte (8 bits plus parity), random word (18 bits), sequential byte (8 bits plus parity) and long word (4 bytes plus 4 parity bits) is possible. Address generation, flag calculation logic and byte parity error detection logic are provided on chip. Data can be passed to and from each Port in a "Flow Through" mode. Programmable break points are available for automatic "retransmit" and "rewrite" functions. In addition, a full complimentary set of status flags is featured for external monitoring. A 120-Pin PGA Package is used.

The SSL72432 is quite similar to the SSL72436 in structure and functions, except for the fact that there are no parity bits and that the buses are only 32 bits wide. A small number of flags and the "Flow Through" mode has been eliminated in this version. Choices of package are 84-Pin PGA and 84-Pad PLCC.

Packaged in an industry standard 68-Pin PGA and PLCC, the SSL72434 has a subset of the SSL72436 functions, size and bus width. The memory array consists of two 128 x 18 bit structures. Port Q data bus is 18 bits wide while Port P is selectable as 9 bits or 18 bits wide. Both buses are Bi-Directional.

The SSL72435 has a subset of functions, size and flags of the SSL72436. Port P is 18 bits wide and Port Q is 36 bits wide. A 84-Pad PLCC and a 84-Pin PGA will be available for this device.

FUNCTIONAL BLOCK DIAGRAM

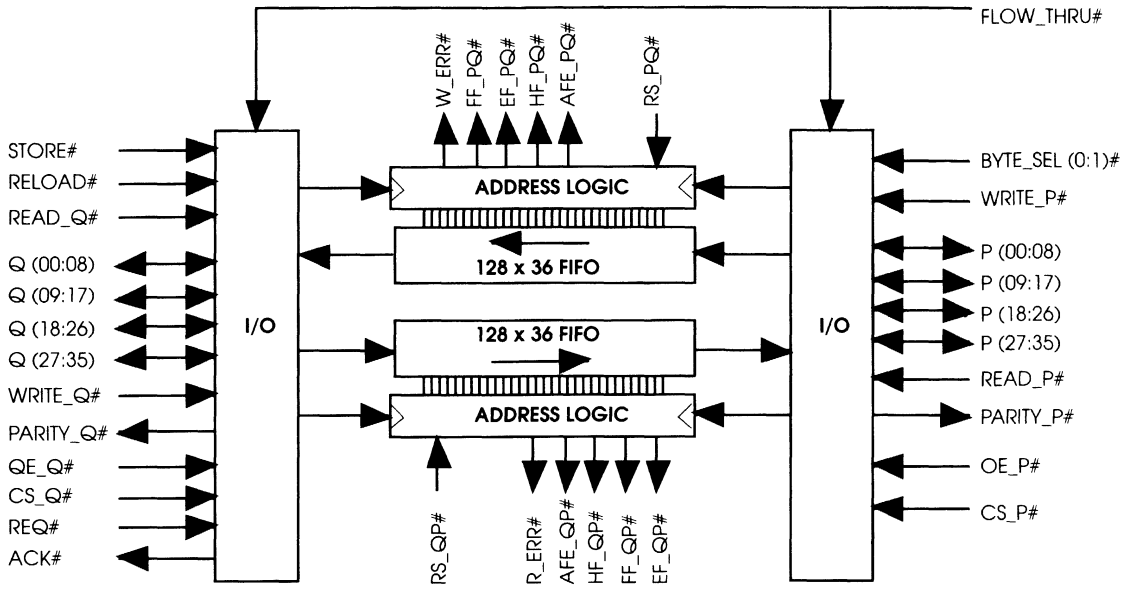


Figure 1. Functional Block Diagram of SSL72436: 128 x 36 Bi-Directional FIFO

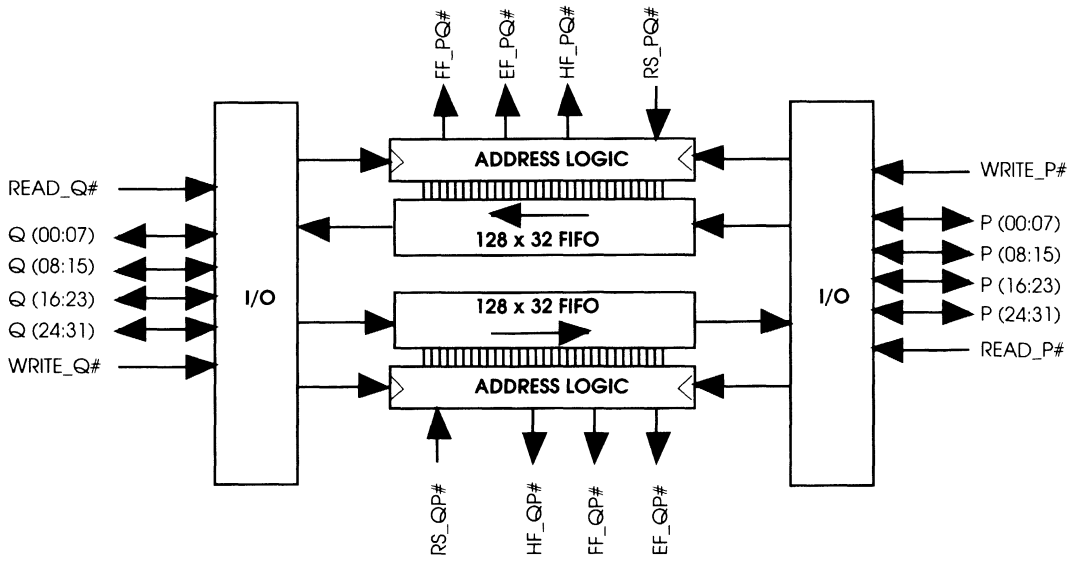


Figure 2. Functional Block Diagram of SSL72432: 128 x 32 Bi-Directional FIFO

FUNCTIONAL BLOCK DIAGRAM

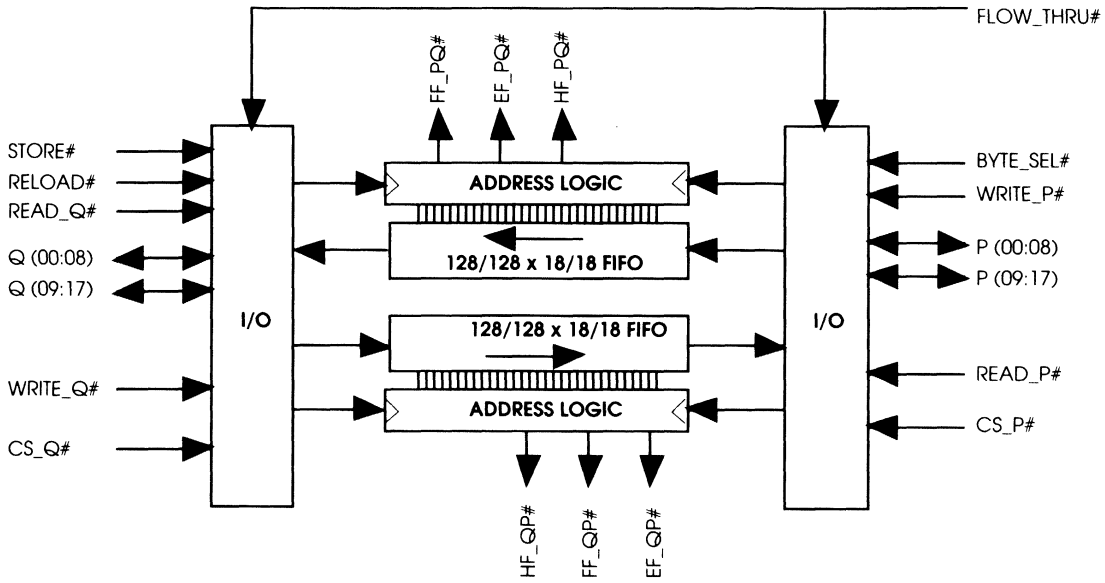


Figure 3. Functional Block Diagram of SSL72434: 128/128 x 18/9 Bi-Directional FIFO

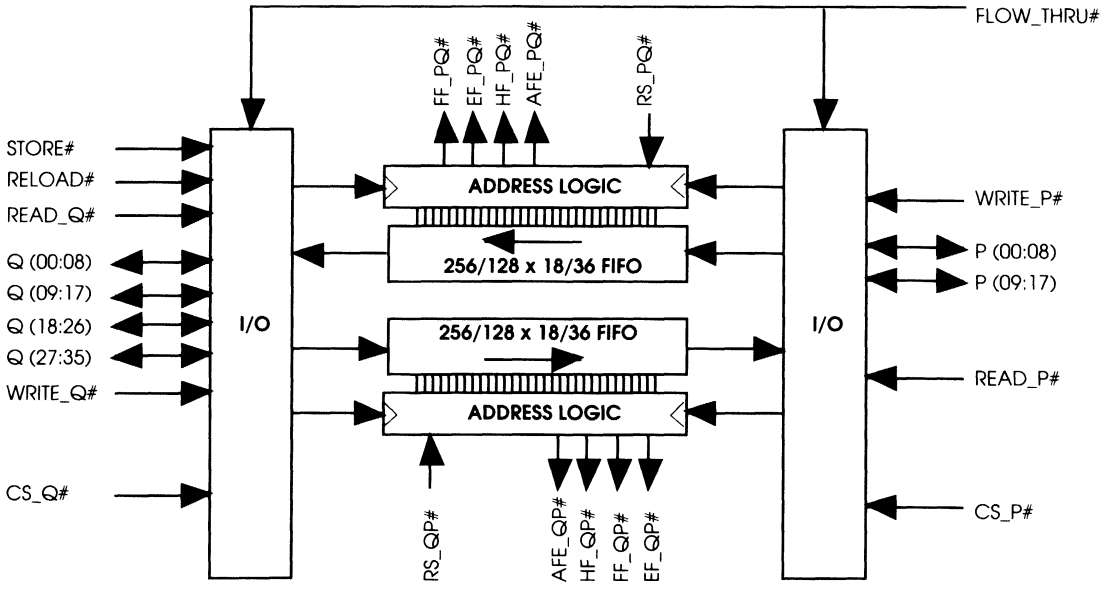


Figure 4. Functional Block Diagram of SSL72435: 128/256 x 36/18 Bi-Directional FIFO

FEATURES SUMMARY

Feature	SSL72436	SSL72432	SSL72434	SSL72435	NOTES
Port P Data I/O Pins	36/18/9	32	18/9	18/9	
Port P: Write and Read	YES	YES	YES	YES	
Port P Chip Select CS (System Clock)	YES	NO	YES	YES	1
Port P Output Enable OE Control	YES	*	*	*	1
Port P Byte Select Pins	YES	*	*	YES	
Port Q Data I/O Pins	36/18/9	32	18/9	18/9	
Port Q: Write and Read	YES	YES	YES	YES	
Port Q Chip Select CS (System Clock)	YES	NO	YES	YES	1
Port Q Output Enable OE Control	YES	*	*	*	
Port Q Store and Reload	YES	NO	YES	YES	
Port Byte Parity error Pins	YES	NO	NO	NO	
Flags: Full, Empty	YES	YES	YES	YES	
Flag: Almost Full/Empty	YES	NO	YES	NO	
Flag: Half Full	YES	YES	YES	YES	
Flag: Reload Error	YES	NO	NO	NO	
Independent Reset Pins	YES	YES	YES	NO	2
Flow Through Mode select	YES	**	YES	**	
Request, Aknowledge Handshake Pins	YES	NO	NO	NO	1
Programmable HF and AFE Flags	*	*	*	*	
Packages	PGA	PLCC, PGA	PLCC, PGA	PLCC, PGA	
Pin Count	120	84	68	84	

NOTES:
(1) This function is programmable during RESET using Data Pins.
(2) This function is only possible during RESET.

BiCMOS TTL LOGIC

Saratoga Semiconductor

SSL29660

32-Bit BiCMOS TTL Error Detection & Correction Unit

PRELIMINARY INFORMATION

FEATURES

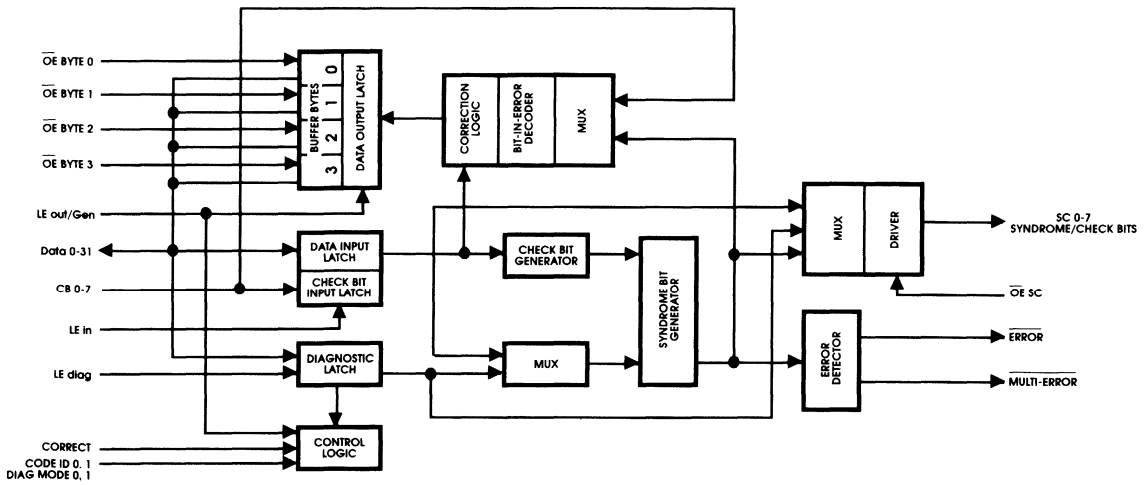
- **High Speed Error Detection & Correction**
  16ns Detection
  24ns Correction
- **Expanded Functionality**
  Cascadeable to Form 64-Bit Word
  Single Bit Correction
  All Double & Some Triple Bit Detection
- **Full Military Temperature Range**
- **68-pin PGA, LCC, and PLCC Packages**
- **Pin Compatible with Industry Standard**
  AMD29660
  IDT49C46B
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

The SSL29660 is a single chip 32-bit Error Detection and Correction Unit (EDAC) with TTL input and output compatibility. It generates check bits on a 32-bit data field according to a modified Hamming code, and corrects the data word when the check bits are supplied. Operating on data fetched from the main memory, the EDAC detects all single-bit errors. Seven check bits are used with each 32-bit word.

Two diagnostic modes are featured, in which diagnostic data can be loaded into the chip to simplify device testing and to execute system level diagnostics functions. In a single chip, the EDAC provides the necessary memory error detection and correction capability required to protect data integrity for large systems. This device is intended for applications in high performance superminicomputers, workstation, RISC-based system and Artificial Intelligence (AI) systems.

FUNCTIONAL BLOCK DIAGRAM



July 1988

BiCMOS TTL MODULES

Saratoga Semiconductor

SSB91256

256K 32,768 Words by 8 Bits BiCMOS TTL Static RAM Module

PRELIMINARY INFORMATION

FEATURES

- **Fast Access Times**
  25/30/35ns max
- **JEDEC Standard 28-pin 600 MIL DIP Package**
- **Plug-in Performance Upgrade**
  Standard 32K x 8 Monolithic
  IDT7M856S Module
- **High Speed Chip-On-Board Technology**
  Higher performance & Cooler Operation
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

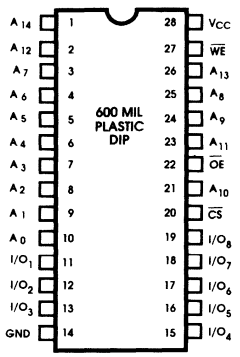
The SSB91256 is a very high speed 256K-bit static RAM module configured as 32,768 words by 8 bits. Four SSM7198 die (16K x 4) are incorporated in this 28-pin, JEDEC standard 600 MIL plastic DIP. Proven and reliable "Chip-On-Board" packaging techniques on an FR4 substrate are employed in the construction of the module. The SSB91256 is a direct speed upgrade of the industry and JEDEC standard pin-out of the monolithic 256K static RAM (32K x 8 bits organization).

A high speed inverter interprets the higher order address (A_{14}) to select two of the four 16K x 4 SRAMs. For the commercial temperature range of 0°C to 70°C and with V_{CC} = 5V ±10%, maximum access time of 25ns is achieved. 30ns and 35ns versions are also available.

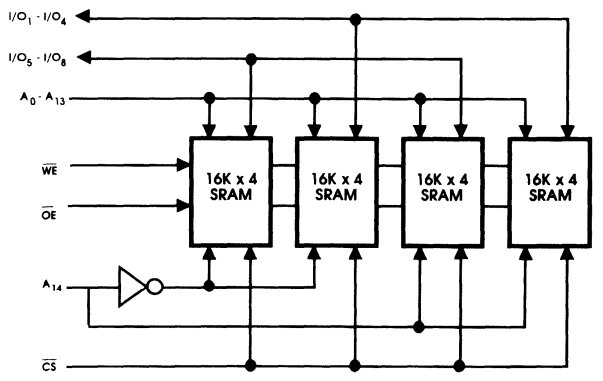
Power consumption for this module at all speeds is 3.2 W. Lower standby power of 320 mW is achieved when the chip select signal ($\overline{CS}$) is inactive or in logic high state. The combination of fast access time and low power consumption is made possible by the use of Saratoga Semiconductor's propretary BiCMOS SABiC process technology.

The high speed SRAM module is intended for applications in computers and workstations as cache memory, writeable control store, look-up table and a variety of buffering purposes.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



July 1988

Saratoga Semiconductor

SSB91257/8/9

256K 16,384 Words by 16 Bits BiCMOS TTL Static RAM Module

PRELIMINARY INFORMATION

FEATURES

- **Fast Access Times**
  20/25/30ns max
- **High Density Plastic 40-Pin SIP & ZIP Modules**
- **Multiple Configurations for Flexibility**
  SSB91257: Common I/O
  SSB91258: Common I/O with OE
  SSB91259: Common I/O with OE and Two CS
- **High Speed Chip-On-Board Technology**
  Higher Performance & Cooler Operation
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

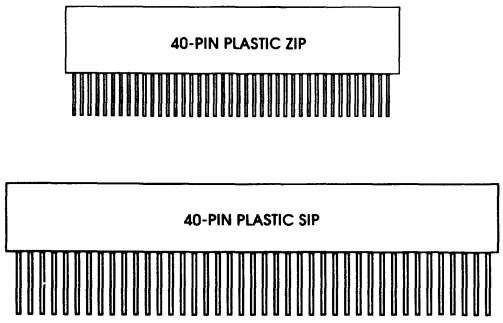
The SSB91257/91258/91259 are very high speed 256K-bit static RAM modules, configured as 16,384 by 16 bits. The SSB91257/91258/91259 incorporate four SSM7166/7188/7198 die (16K x 4) respectively. Proven and reliable "Chip-On-Board" packaging techniques and epoxy laminate FR4 substrates are used in the construction of these modules.

No on-module decoder is needed to attain maximum speed equalling that of the monolithic chip. For the commercial temperature range of 0°C to 70°C and with V_{CC}= 5V ±10%, maximum access time of 20ns is achieved. 25ns and 30ns versions are also available. Due to the unique construction of these modules, they operate cooler and dissipate power evenly across the surfaces of the module.

Power consumption for these modules at all speeds is 3.2 W. Lower standby power of 320 mW is achieved when the chip select signal ($\overline{CS}$) is inactive or in logic high state. The combination of fast access time and low power consumption is made possible by the use of Saratoga Semiconductor's propretary BiCMOS SABiC process technology.

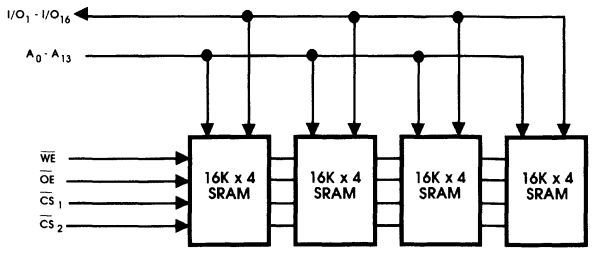
These high speed SRAM modules are intended for applications in computers and workstations as cache memory, writeable control store, look-up table and a variety of buffering purposes. With their tight geometry and thin profile, these modules provide 5X (SIP) and 10X (ZIP) the memory density on a given area of the printed circuit when compared to the equivalent DIP configuration.

PIN CONFIGURATION



Note: Pin-out assignment to be determined.

FUNCTIONAL BLOCK DIAGRAM



Note: $\overline{CS}_1$ and $\overline{CS}_2$ are for SSB91259 only; $\overline{CS}_1$ is for SSB91257 and SSB91258; $\overline{OE}$ is for SSB91257 and SSB91259.

July 1988

Saratoga Semiconductor

SSB91260

256K 16,384 Words by 16 Bits BiCMOS TTL Static RAM Module

PRELIMINARY INFORMATION

FEATURES

- **Fast Access Times**
  20/25/30ns max
- **High Density Plastic 40-Pin SIP Module**
- **Fully Compatible with IDT8MP656S**
- **High Speed Chip-On-Board Technology**
  Higher Performance & Cooler Operation
- **16-Bit Word Width**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

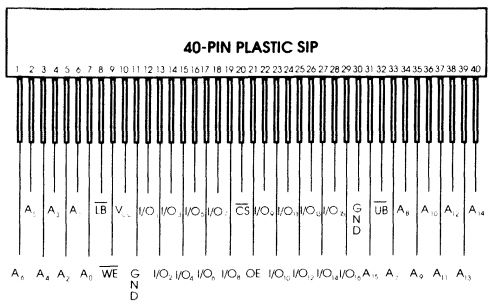
The SSB9160 is a very high speed 256K-bit static RAM module, configured as 16,384 by 16 bits. The SSB91260 incorporates four SSM7198 die (16K x 4) and is fully compatible with yet faster than the IDT8MP656S module. Proven and reliable "Chip-On-Board"packaging techniques and epoxy laminate FR4 substrates are used in the construction of this module.

No on-module decoder is needed to attain maximum speed equalling that of the monolithic chip. For the commercial temperature range of 0°C to 70°C and with V_{CC} = 5V ±10%, maximum access time of 20ns is achieved. 25ns and 30ns versions are also available. Due to the unique construction of these modules, they operate cooler and dissipate power evenly across the surfaces of the module.

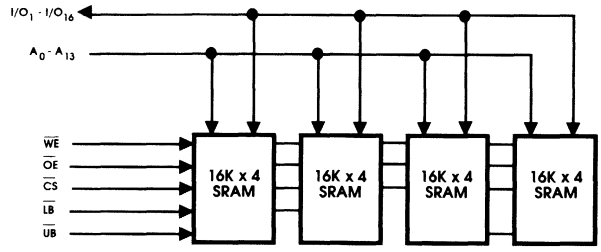
Power consumption for this module at all speeds is 3.2 W. Lower standby power of 320 mW is achieved when the chip select signal ($\overline{CS}$) is inactive or in logic high state. The combination of fast access time and low power consumption is made possible by the use of Saratoga Semiconductor's propretary BiCMOS SABiC process technology.

This high speed SRAM module is intended for applications in computers and workstations as cache memory,writeable control store, look-up table and a variety of buffering purposes. With its tight geometry and thin profile, this module provides 5X the memory density on a given area of the printed circuit board when compared to the equivalent DIP configuration.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



July 1988

Saratoga Semiconductor

SSB91512/3/4

512K of x8, x16, x32 Bits BiCMOS TTL Static RAM Module

PRELIMINARY INFORMATION

FEATURES

- **Fast Access Times**
  20/25/30ns max
- **High Density Plastic 60-Pin ZIP Modules**
- **Multiple Configurations for Flexibility**
  SSB91512: Common I/O
  SSB91513: Common I/O with OE
  SSB91514: Common I/O with OE and Two CS
  Each Configurable as x8, x16, x32 Bits
- **512K Bits of Customer Configurable SRAM**
- **High Speed Chip-On-Board Technology**
  Higher Performance & Cooler Operation
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

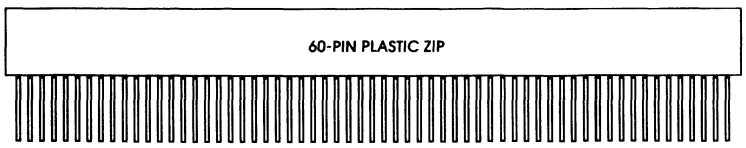
The SSB91512/91513/91514 are very high speed 512K-bit static RAM modules customer configured as 8, 16, or 32 bits. The SSB915127/91513/91514 incorporate eight SSM-7166/7188/7198 die (16K x 4) respectively in a 60-pin plastic Zip package. Proven and reliable "Chip-On-Board" packaging techniques and epoxy laminate FR4 substrates are used in the construction of these modules.

No on-module decoder is needed in the 32-bit configuration to attain maximum speed equalling that of the monolithic chip. For the commercial temperature range of 0°C to 70°C and with V_{CC}= 5V ±10%, maximum access time of 20ns is achieved. 25ns and 30ns versions are also available. The x8 and x16 options will be 5-10ns slower depending upon the type of decoder chosen by the system designer. Due to the unique construction of these modules, they operate cooler and dissipate power evenly across the surfaces of the module.

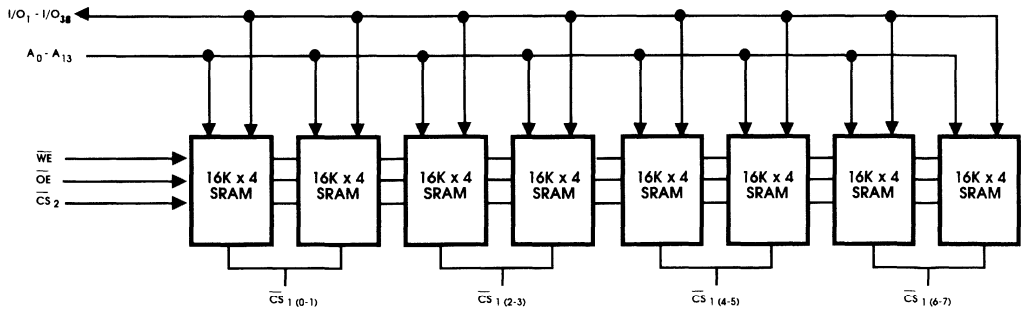
Power consumption for these modules at all speeds is 6.4 W. Lower standby power of 640 mW is achieved when the chip select signal (CS) is inactive or in logic high state. The combination of fast access time and low power consumption is made possible by the use of Saratoga Semiconductor's propretary BiCMOS SABiC process technology.

These high speed SRAM modules are intended for applications in computers and workstations as cache memory, writeable control store, look-up table and a variety of buffering purposes. With their tight geometry and thin profile, these modules provide 10X the memory density on a given area of the printed circuit board when compared to the equivalent DIP configuration.

PIN CONFIGURATION



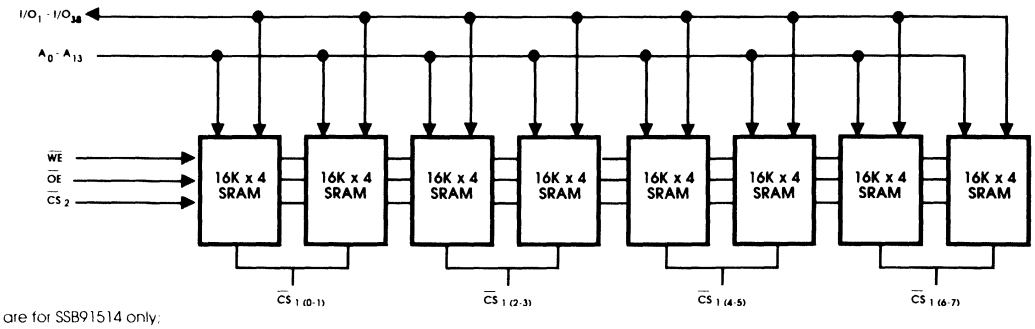
FUNCTIONAL BLOCK DIAGRAM



Note: $\overline{CS}_1$ and $\overline{CS}_2$ are for SSB91514 only;
$\overline{OE}$ is for SSB91512 and SSB91514;
$\overline{CS}_1$ is for SSB91512 and SSB91513;
Pin-out assignment to be determined.

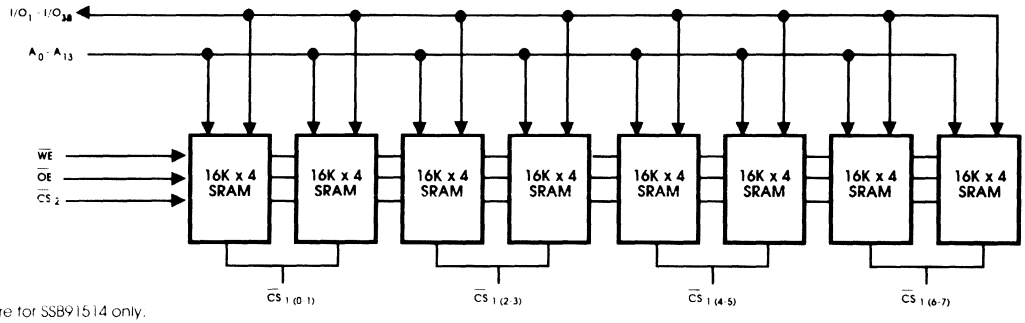
July 1988

x32



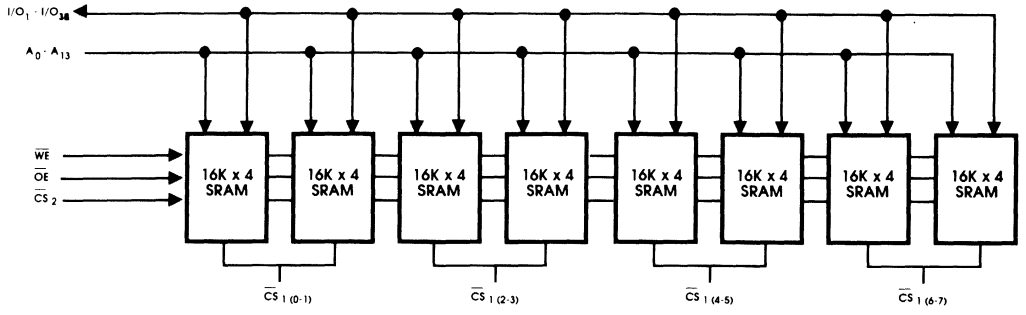
Note: $\overline{CS}_1$ and $\overline{CS}_2$ are for SSB91514 only;
$\overline{OE}$ is for SSB91512 and SSB91514;
$\overline{CS}_1$ is for SSB91512 and SSB91513.

x16



Note: $\overline{CS}_1$ and $\overline{CS}_2$ are for SSB91514 only;
$\overline{OE}$ is for SSB91512 and SSB91514;
$\overline{CS}_1$ is for SSB91512 and SSB91513.

x8



Note: $\overline{CS}_1$ and $\overline{CS}_2$ are for SSB91514 only;
$\overline{OE}$ is for SSB91512 and SSB91514;
$\overline{CS}_1$ is for SSB91512 and SSB91513.

BiCMOS ECL SRAMS

Saratoga Semiconductor

SSM100470

4K 4,096 Words by 1 Bit BiCMOS ECL Static RAM

FEATURES

- **Fast Access Times**
  SSM100470-10: 10ns Address Access
  6ns Chip Select Access
  SSM100470-15: 15ns Address Access
  8ns Chip Select Access
- **Fully Compatible with 100K Families**
  Voltage Compensated
  Temperature Compensated
- **Industry Standard DIP Package**
- **Pin Compatible with Industry Standard**
  MBM100470
  HM100470
  μPB1002470
- **Low Power Consumption – 195 mA**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature range Capability

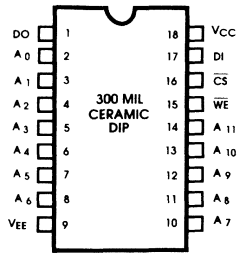
DESCRIPTION

The SSM100470 is a high performance 100K ECL static RAM organized 4,096 words by 1 bit. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input ($\overline{CS}$) to its active low condition. When $\overline{CS}$ is low and the Write Enable input ($\overline{WE}$) is also low, information on the Data Input (DI) is written into the memory cell specified by the 12 bit address placed on the Address Inputs (A_0-A_{11}). With $\overline{CS}$ low and $\overline{WE}$ high, the content of the addressed memory cell is transferred to the Data Output (DO). This output is in the emitter-follower configuration to permit full wire-ORing capability.

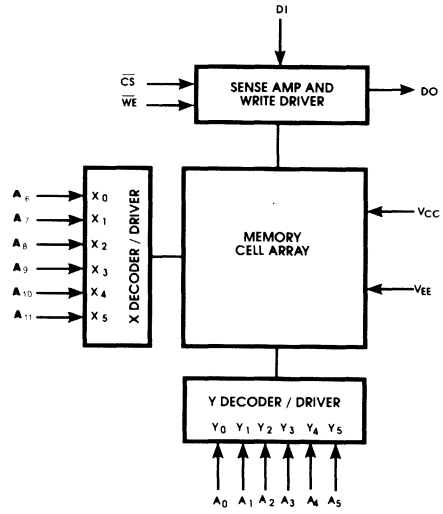
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{11}	Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
DI	Data Input
DO	Data Output
V_{CC}, V_{EE}	Power Supply Pins

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	DI	DO
Read	L	H	X	DO
Write '0'	L	L	L	L
Write '1'	L	L	H	L
Disabled	H	X	X	L

H = High Voltage Level X = Irrelevant L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Supply Voltage (V_{EE} to GND)	V_{EE}	+0.5	-7.0	V
Input Voltage	V_{IN}	+0.5	V_{EE}	V
Output Current (DC, Output High)	I_{OUT}		-30	mA
Temperature Under Bias	T_A for DIP	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Supply Voltage [1]	V_{EE}	-5.7	-4.5	-4.2	V
Ambient Temperature	T_A	0		+85	°C

[1] V_{EE} referenced to V_{CC}

DC CHARACTERISTICS [2]

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE MIN	VALUE MAX	UNIT
V_{OH}	Output High Voltage	V_{IN} = V_{IH} max or V_{IL} min	-1025	-880	mV
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} max or V_{IL} min	-1810	-1620	mV
V_{OHC}	Output High Voltage	V_{IN} = V_{IH} min or V_{IL} max	-1035		mV
V_{OLC}	Output Low Voltage	V_{IN} = V_{IH} min or V_{IL} max		-1610	mV
V_{IH}	Input High Voltage	Guaranteed input voltage high for all inputs	-1165	-880	mV
V_{IL}	Input Low Voltage	Guaranteed input voltage low for all inputs	-1810	-1475	mV
I_{IH}	Input High Current	V_{IN} = V_{IH} max		220	µA
I_{IL}	Input Low Current	V_{IN} = V_{IL} min	-50		µA
I_{IL}	$\overline{CS}$ Input Low Current	V_{IN} = V_{IL} min	0.5	170	µA
I_{EE}	Power Supply Current	All inputs and outputs open	-195		mA

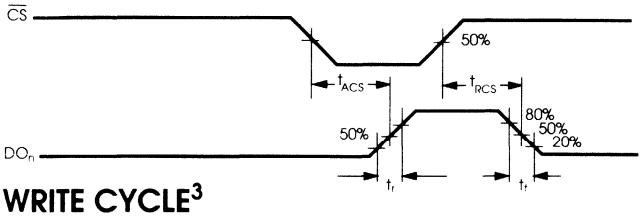
[2] V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V and 30 pF to GND
T_A = 0 °C to 85 °C for DIP, Airflow ≥ 2.5 m/s

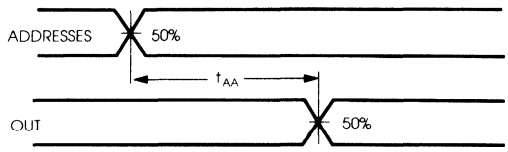
AC CHARACTERISTICS

READ CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM100470-10 MIN	SSM100470-10 MAX	SSM100470-15 MIN	SSM100470-15 MAX	UNIT
Address Access Time	t_{AA}		10		15	ns
Chip Select Recovery Time	t_{ACS}		6		8	ns
Chip Select Access Time	t_{RCS}		6		8	ns

READ CYCLE TIMING DIAGRAMS [4]

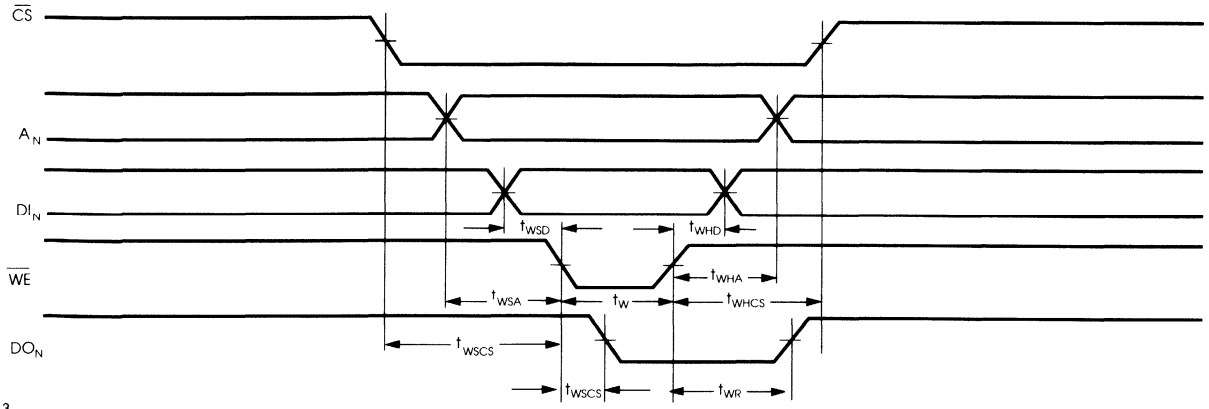




WRITE CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM100470-10 MIN	SSM100470-10 MAX	SSM100470-15 MIN	SSM100470-15 MAX	UNIT
Write Pulse Width	t_W	10		15		ns
Write Disable Time	t_{WS}		6		8	ns
Write Recovery Time	t_{WR}		10		15	ns
Address Set Up Time	t_{WSA}	2		2		ns
Chip Select Set Up Time	t_{WSCS}	2		2		ns
Data Set Up Time	t_{WSD}	2		2		ns
Address Hold Time	t_{WHA}	1		2		ns
Chip Select Hold Time	t_{WHCS}	1		2		ns
Data Hold Time	t_{WHD}	1		2		ns

WRITE CYCLE TIMING DIAGRAM [4]



[3] V_{CC} = 0V, V_{EE} = -4.5V ±5%, T_A = 0 °C to 85 °C, Output Load = 50Ω to -2.0V and 30pF to GND, Airflow ≥ 2.5 m/s.
[4] All timing measurements referenced to 50% input levels.

OUTPUT RISE AND FALL TIME • CAPACITANCE • AC TEST CONDITIONS

PARAMETER	SYMBOL	VALUE TYP	VALUE MAX	UNIT
Output Rise Time	t_r	2.5		ns
Output Fall Time	t_f	2.5		ns
Input Pin Capacitance	C_{IN}	4		pF
Output Pin Capacitance	C_{OUT}	6		pF

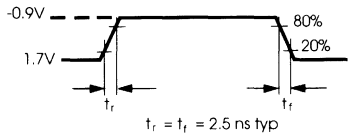


Figure A
Input Pulse Conditions

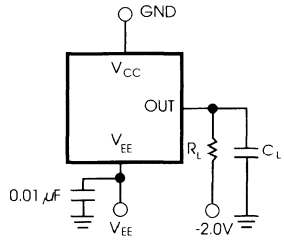
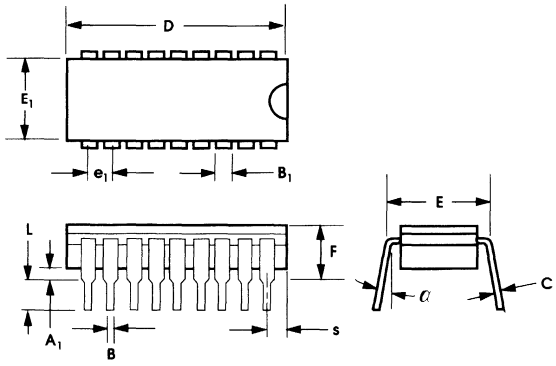


Figure B
Load Circuit

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including probe and stray capacitance)

PACKAGE DIMENSIONS



18 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.045
B	.014	.023
B_1	.050	.065
C	.009	.015
D		.920
E	.300	.320
E_1	.285	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	TEMPERATURE RANGE MAX	TEMPERATURE RANGE UNIT
SSM100470-10CC	10ns	20-Pin CERDIP	0	+85	°C
SSM100470-15CC	15ns	20-Pin CERDIP	0	+85	°C

NOTE: PLEASE CONTACT FACTORY for information regarding LCC, FLATPACK, and MILITARY TEMPERATURE RANGE devices.

Saratoga Semiconductor

SSM100474

4K 1,024 Words by 4 Bits BiCMOS ECL Static RAM

FEATURES

- **Fast Access Times**
  SSM100474-8: 8ns Address Access
  5ns Chip Select Access
  SSM100474-10: 10ns Address Access
  6ns Chip Select Access
  SSM100474-15: 15ns Address Access
  8ns Chip Select Access
- **Fully Compatible with 100K Families**
  Voltage Compensated
  Temperature Compensated
- **Industry Standard DIP Package**
- **Pin Compatible with Industry Standard**
  MBM100474
  HM100474
  μPB100474
- **Low Power Consumption – 240 mA**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

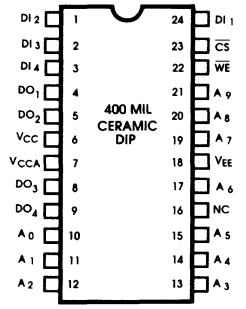
DESCRIPTION

The SSM100474 is a high performance 100K ECL static RAM organized 1,024 words by 4 bits. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input ($\overline{CS}$) to its active low condition. When $\overline{CS}$ is low and the Write Enable input ($\overline{WE}$) is also low, information on the Data Inputs (DI_1 - DI_4) is written into the memory cell specified by the 10 bit address placed on the Address Inputs (A_0-A_9). With $\overline{CS}$ low and $\overline{WE}$ high, the content of the addressed memory cell is transferred to the Data Outputs (DO_1- DO_4). This output is in the emitter-follower configuration to permit full wire-ORing capability.

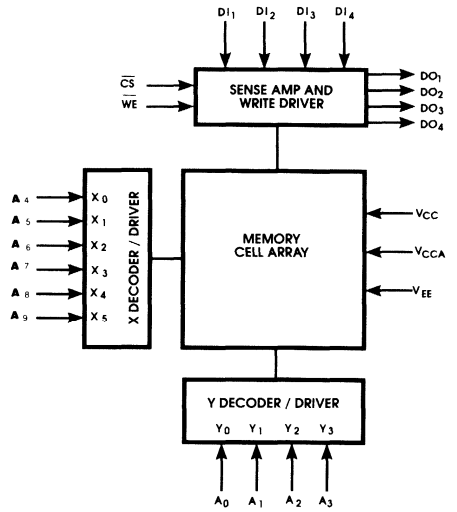
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_9	Address Inputs
DI_1 - DI_4	Data Inputs
DO_1 - DO_4	Data Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
V_{CC}, V_{CCA}, V_{EE}	Power Supply Pins
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	DI n	DO n
Read	L	H	X	DO
Write '0'	L	L	L	L
Write '1'	L	L	H	L
Disabled	H	X	X	L

H = High Voltage Level X = Irrelevant L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Supply Voltage (V_{EE} to GND)	V_{EE}	+0.5	-7.0	V
Input Voltage	V_{IN}	+0.5	V_{EE}	V
Output Current (DC, Output High)	I_{OUT}		-30	mA
Temperature Under Bias	T_A for DIP	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Supply Voltage [1]	V_{EE}	-5.7	-4.5	-4.2	V
Ambient Temperature	T_A	0		+85	°C

[1] V_{EE} referenced to V_{CC} .

DC CHARACTERISTICS [2]

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE MIN	VALUE MAX	UNIT
V_{OH}	Output High Voltage	V_{IN} = V_{IH} max or V_{IL} min	-1025	-880	mV
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} max or V_{IL} min	-1810	-1620	mV
V_{OHC}	Output High Voltage	V_{IN} = V_{IH} min or V_{IL} max	-1035		mV
V_{OLC}	Output Low Voltage	V_{IN} = V_{IH} min or V_{IL} max		-1610	mV
V_{IH}	Input High Voltage	Guaranteed input voltage high for all inputs	-1165	-880	mV
V_{IL}	Input Low Voltage	Guaranteed input voltage low for all inputs	-1810	-1475	mV
I_{IH}	Input High Current	V_{IN} = V_{IH} max		220	µA
I_{IL}	Input Low Current	V_{IN} = V_{IL} min	-50		µA
I_{IL}	$\overline{CS}$ Input Low Current	V_{IN} = V_{IL} min	0.5	170	µA
I_{EE}	Power Supply Current	All inputs and outputs open	-240		mA

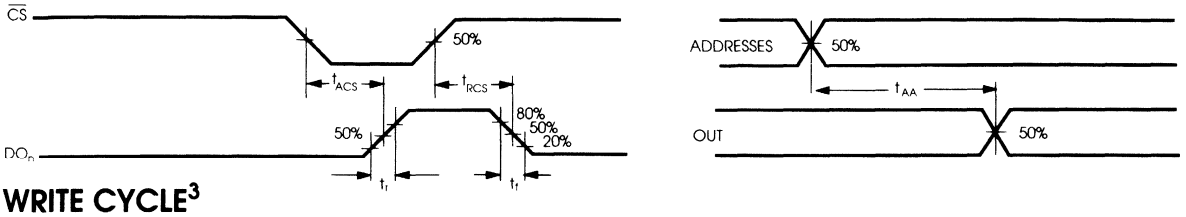
[2] V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V and 30 pF to GND
T_A = 0 °C to 85 °C for DIP, Airflow ≥ 2.5 m/s

AC CHARACTERISTICS

READ CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM100474-8 MIN	SSM100474-8 MAX	SSM100474-10 MIN	SSM100474-10 MAX	SSM100474-15 MIN	SSM100474-15 MAX	UNIT
Address Access Time	t_{AA}		8		10		15	ns
Chip Select Recovery Time	t_{ACS}		5		6		8	ns
Chip Select Access Time	t_{RCS}		5		6		8	ns

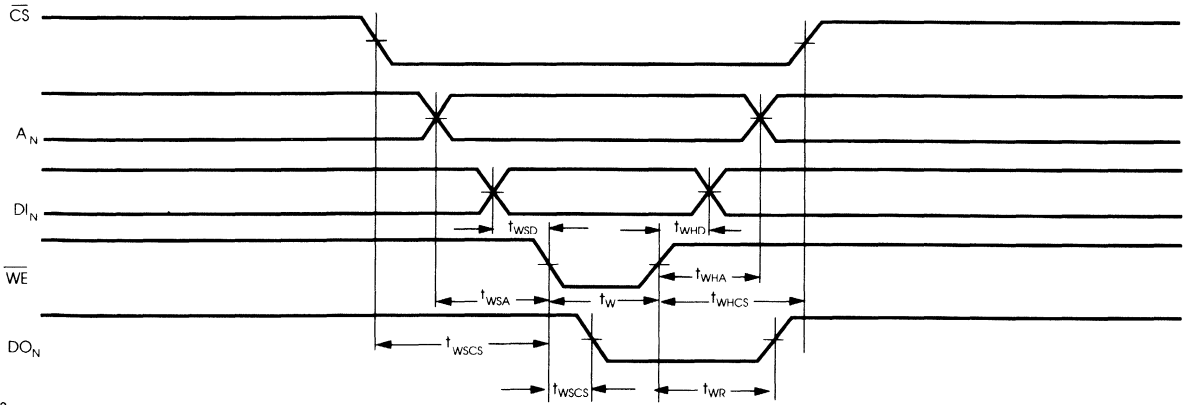
READ CYCLE TIMING DIAGRAMS [4]



WRITE CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM100474-8 MIN	SSM100474-8 MAX	SSM100474-10 MIN	SSM100474-10 MAX	SSM100474-15 MIN	SSM100474-15 MAX	UNIT
Write Pulse Width	t_W	6		8		11		ns
Write Disable Time	t_{WS}		5		6		8	ns
Write Recovery Time	t_{WR}		8		10		15	ns
Address Set Up Time	t_{WSA}	1		1		2		ns
Chip Select Set Up Time	t_{WSCS}	1		1		2		ns
Data Set Up Time	t_{WSD}	1		1		2		ns
Address Hold Time	t_{WHA}	1		1		2		ns
Chip Select Hold Time	t_{WHCS}	1		1		2		ns
Data Hold Time	t_{WHD}	1		1		2		ns

WRITE CYCLE TIMING DIAGRAM [4]



[3] V_{CC} = 0V, V_{EE} = -4.5V ±5%, T_A = 0 °C to 85 °C, Output Load = 50Ω to -2.0V and 30pF to GND, Airflow ≥2.5 m/s.
[4] All timing measurements referenced to 50% input levels.

OUTPUT RISE AND FALL TIME • CAPACITANCE • AC TEST CONDITIONS

PARAMETER	SYMBOL	VALUE TYP	VALUE MAX	UNIT
Output Rise Time	t_r	2.5		ns
Output Fall Time	t_f	2.5		ns
Input Pin Capacitance	C_{IN}	4		pF
Output Pin Capacitance	C_{OUT}	6		pF

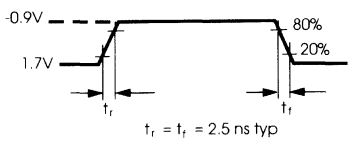


Figure A
Input Pulse Conditions

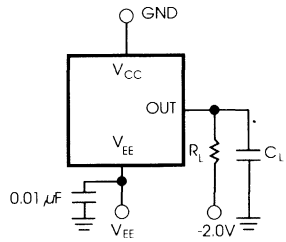
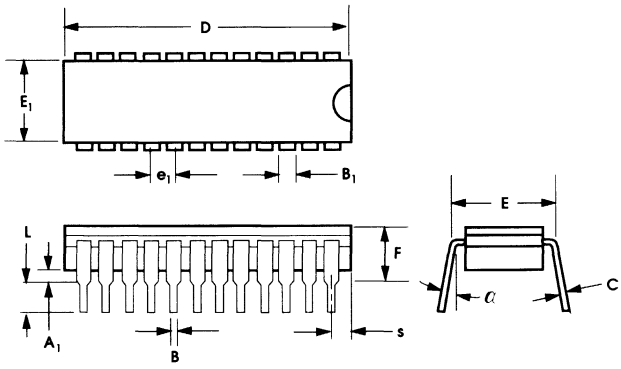


Figure B
Load Circuit

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including probe and stray capacitance)

PACKAGE DIMENSIONS



24 LEAD 400 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.250
E	.380	.420
E_1	.350	.410
e_1	.090	.110
F		.225
L	.125	.200
s		.070
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM100474-10CC	10ns	20-Pin CERDIP	0	+85	°C
SSM100474-15CC	15ns	20-Pin CERDIP	0	+85	°C

NOTE: PLEASE CONTACT FACTORY for information regarding LCC, FLATPACK, and MILITARY TEMPERATURE RANGE devices.

Saratoga Semiconductor

SSM100480

16K 16,384 Words by 1 Bit BiCMOS ECL Static RAM

FEATURES

- **Fast Access Times**
  SSM100480-10: 10ns Address Access
  5ns Chip Select Access
  SSM100480-15: 15ns Address Access
  8ns Chip Select Access
- **Fully Compatible with 100K Families**
  Voltage Compensated
  Temperature Compensated
- **Industry Standard DIP Package**
- **Pin Compatible with Industry Standard**
  MBM100480
  HM100480
  μPB100480
- **Low Power Consumption – 195 mA**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

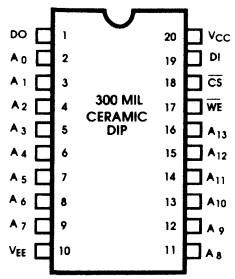
DESCRIPTION

The SSM100480 is a high performance 100K ECL static RAM organized 16,384 words by 1 bit. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input ($\overline{CS}$) to its active low condition. When $\overline{CS}$ is low and the Write Enable input ($\overline{WE}$) is also low, information on the Data Input (DI) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0-A_{13}). With $\overline{CS}$ low and $\overline{WE}$ high, the content of the addressed memory cell is transferred to the Data Output (DO). This output is in the emitter-follower configuration to permit full wire-ORing capability.

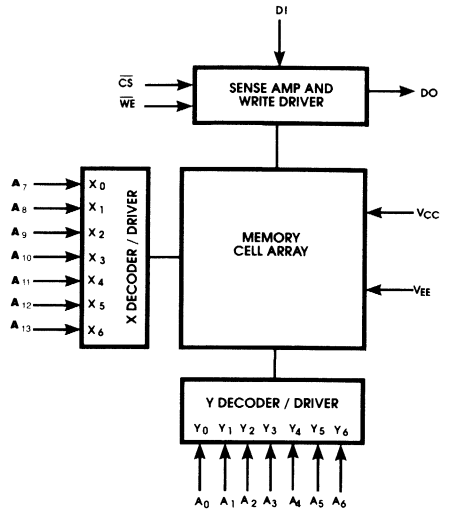
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{13}	Address Inputs
DI	Data Input
DO	Data Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}, V_{EE}	Power Supply Pins

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	DI	DO
Read	L	H	X	DO
Write '0'	L	L	L	L
Write '1'	L	L	H	L
Disabled	H	X	X	L

H = High Voltage Level X = Irrelevant L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Supply Voltage (V_{EE} to GND)	V_{EE}	+0.5	-7.0	V
Input Voltage	V_{IN}	+0.5	V_{EE}	V
Output Current (DC, Output High)	I_{OUT}		-30	mA
Temperature Under Bias	T_A for DIP	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Supply Voltage [1]	V_{EE}	-5.7	-4.5	-4.2	V
Ambient Temperature	T_A	0		+85	°C

[1] V_{EE} referenced to V_{CC}

DC CHARACTERISTICS [2]

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE MIN	VALUE MAX	UNIT
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	-1025	-880	mV
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	-1810	-1620	mV
V_{OHC}	Output High Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	-1035		mV
V_{OLC}	Output Low Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max		-1610	mV
V_{IH}	Input High Voltage	Guaranteed input voltage high for all inputs	-1165	-880	mV
V_{IL}	Input Low Voltage	Guaranteed input voltage low for all inputs	-1810	-1475	mV
I_{IH}	Input High Current	$V_{IN} = V_{IH}$ max		220	µA
I_{IL}	Input Low Current	$V_{IN} = V_{IL}$ min	-50		µA
I_{IL}	$\overline{CS}$ Input Low Current	$V_{IN} = V_{IL}$ min	0.5	170	µA
I_{EE}	Power Supply Current	All inputs and outputs open	-195		mA

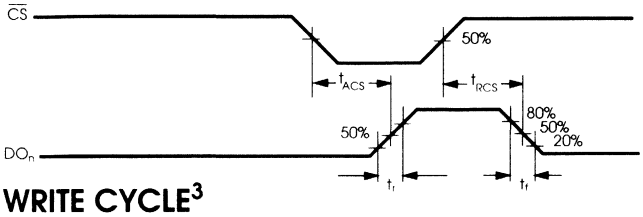
[2] V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V and 30 pF to GND
T_A = 0 °C to 85 °C for DIP, Airflow ≥ 2.5 m/s

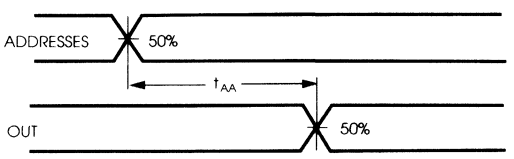
AC CHARACTERISTICS

READ CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM100480-10 MIN	SSM100480-10 MAX	SSM100480-15 MIN	SSM100480-15 MAX	UNIT
Address Access Time	t_{AA}		10		15	ns
Chip Select Recovery Time	t_{ACS}		5		8	ns
Chip Select Access Time	t_{RCS}		5		8	ns

READ CYCLE TIMING DIAGRAMS [4]

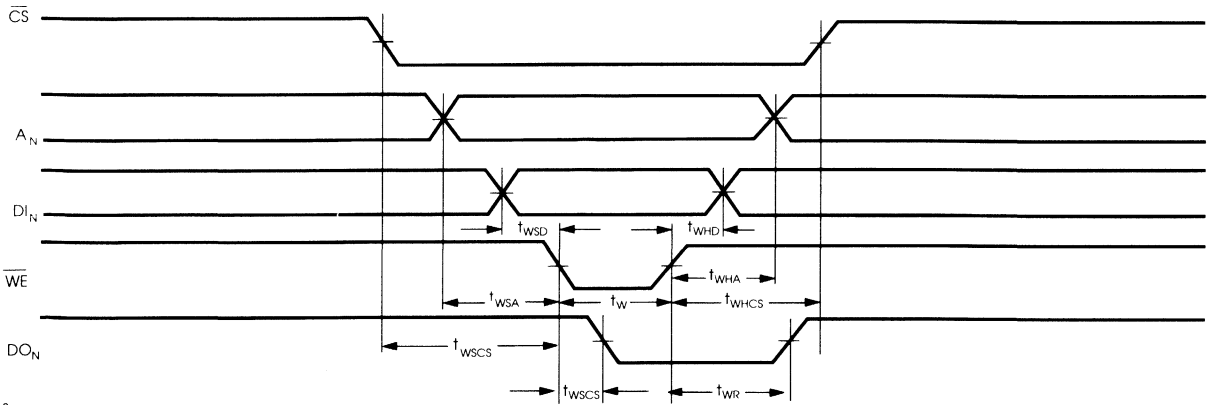




WRITE CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM100480-10 MIN	SSM100480-10 MAX	SSM100480-15 MIN	SSM100480-15 MAX	UNIT
Write Pulse Width	t_W	10		15		ns
Write Disable Time	t_{WS}		5		8	ns
Write Recovery Time	t_{WR}		10		15	ns
Address Set Up Time	t_{WSA}	2		2		ns
Chip Select Set Up Time	t_{WSCS}	2		2		ns
Data Set Up Time	t_{WSD}	2		2		ns
Address Hold Time	t_{WHA}	1		2		ns
Chip Select Hold Time	t_{WHCS}	1		2		ns
Data Hold Time	t_{WHD}	1		2		ns

WRITE CYCLE TIMING DIAGRAM [4]



[3] V_{CC} = 0V, V_{EE} = -4.5V ±5%, T_A= 0 °C to 85 °C, Output Load = 50Ω to -2.0V and 30pF to GND, Airflow ≥ 2.5 m/s.
[4] All timing measurements referenced to 50% input levels.

OUTPUT RISE AND FALL TIME • CAPACITANCE • AC TEST CONDITIONS

PARAMETER	SYMBOL	VALUE TYP	VALUE MAX	UNIT
Output Rise Time	t_r	2.5		ns
Output Fall Time	t_f	2.5		ns
Input Pin Capacitance	C_{IN}	4		pF
Output Pin Capacitance	C_{OUT}	6		pF

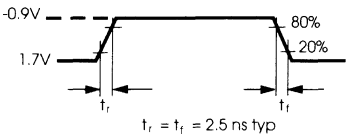


Figure A
Input Pulse Conditions

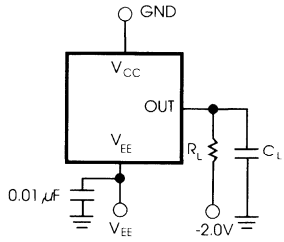
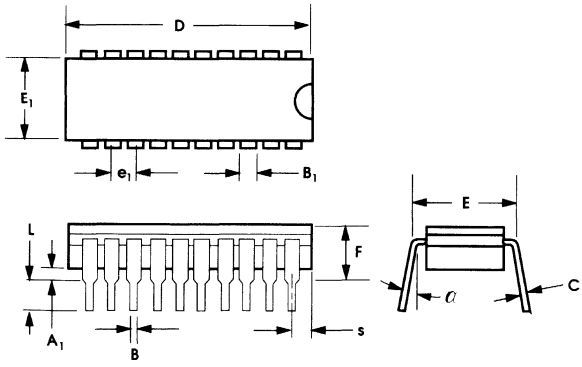


Figure B
Load Circuit

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including probe and stray capacitance)

PACKAGE DIMENSIONS



20 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.060
E	.290	.320
E_1	.220	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
a	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	TEMPERATURE RANGE MAX	UNIT
SSM100480-10CC	10ns	20-Pin CERDIP	0	+85	°C
SSM100480-15CC	15ns	20-Pin CERDIP	0	+85	°C

NOTE: PLEASE CONTACT FACTORY for information regarding LCC, FLATPACK, and MILITARY TEMPERATURE RANGE devices.

Saratoga Semiconductor

SSM100484

16K 4,096 Words by 4 Bits BiCMOS ECL Static RAM

FEATURES

- **Fast Access Times**
  SSM100484-10: 10ns Address Access
  5ns Chip Select Access
  SSM100484-15: 5ns Address Access
  8ns Chip Select Access
- **Fully Compatible with 100K ECL Families**
  Voltage Compensated
  Temperature Compensated
- **Industry Standard DIP Package**
- **Pin Compatible with Industry Standard**
  MBM100484
  HM100484
  μPB100484
- **Low Power Consumption – 220 mA**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

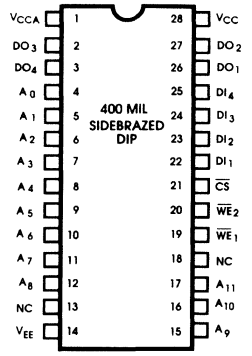
DESCRIPTION

The SSM100484 is a high performance 100K ECL static RAM organized 4,096 words by 4 bits. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input $\overline{CS}$ to its active low condition. When $\overline{CS}$ is low and the two Write Enable inputs ($\overline{WE}_1$ and $\overline{WE}_2$) are also low, information on the Data Inputs (DI_1-DI_4) is written into the memory cell specified by the 12 bit address placed on the Address Inputs (A_0-A_{11}). With $\overline{CS}$ low and $\overline{WE}_1$ or $\overline{WE}_2$ high, the content of the addressed memory cell is transferred to the Data Outputs (DO_1-DO_4). These outputs are in the emitter-follower configuration to permit full wire-ORing capability.

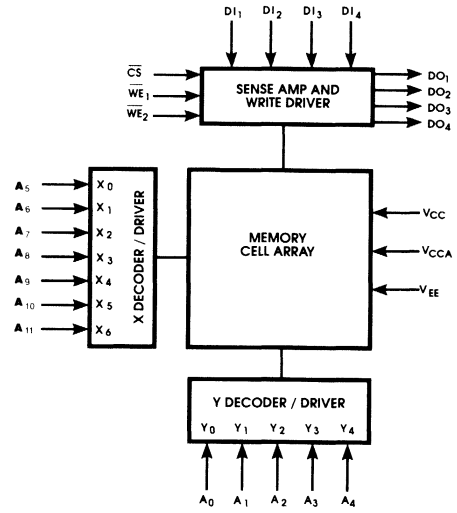
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{11}	Address Inputs
DI_1 - DI_4	Data Inputs
DO_1 - DO_4	Data Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}_1$, $\overline{WE}_2$	Write Enable Inputs
V_{CC}, V_{CCA}, V_{EE}	Power Supply Pins
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}_1$	$\overline{WE}_2$	DI_n	DO_n
Read	L	H	X	X	DO
Read	L	X	H	X	DO
Write '0'	L	L	L	L	L
Write '1'	L	L	L	H	L
Disabled	H	X	X	X	L

H = High Voltage Level X = Irrelevant L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Supply Voltage (V_{EE} to GND)	V_{EE}	+0.5	-7.0	V
Input Voltage	V_{IN}	+0.5	V_{EE}	V
Output Current (DC, Output High)	I_{OUT}		-30	mA
Temperature Under Bias	T_A for DIP	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Supply Voltage[1]	V_{EE}	-5.7	-4.5	-4.2	V
Ambient Temperature	T_A	0		+85	°C

[1] V_{EE} referenced to V_{CC}.

DC CHARACTERISTICS [2]

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE MIN	VALUE MAX	UNIT
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	-1025	-880	mV
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	-1810	-1620	mV
V_{OHC}	Output High Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	-1035		mV
V_{OLC}	Output Low Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max		-1610	mV
V_{IH}	Input High Voltage	Guaranteed input voltage high for all inputs	-1165	-880	mV
V_{IL}	Input Low Voltage	Guaranteed input voltage low for all inputs	-1810	-1475	mV
I_{IH}	Input High Current	$V_{IN} = V_{IH}$ max		220	µA
I_{IL}	Input Low Current	$V_{IN} = V_{IL}$ min	-50		µA
I_{IL}	$\overline{CS}$ Input Low Current	$V_{IN} = V_{IL}$ min	0.5	170	µA
I_{EE}	Power Supply Current	All inputs and outputs open	-220		mA

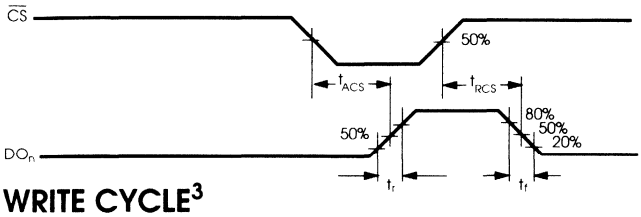
[2] V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V and 30 pF to GND
T_A = 0 °C to 85 °C for DIP, Airflow ≥ 2.5 m/s

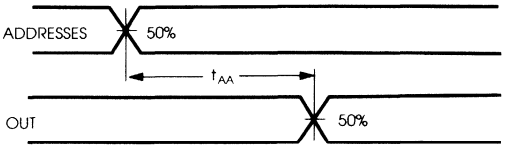
AC CHARACTERISTICS

READ CYCLE[3]

PARAMETER	SYMBOL	VALUE SSM100484-10 MIN	SSM100484-10 MAX	SSM100484-15 MIN	SSM100484-15 MAX	UNIT
Address Access Time	t_{AA}		10		15	ns
Chip Select Recovery Time	t_{ACS}		5		8	ns
Chip Select Access Time	t_{RCS}		5		8	ns

READ CYCLE TIMING DIAGRAMS[4]

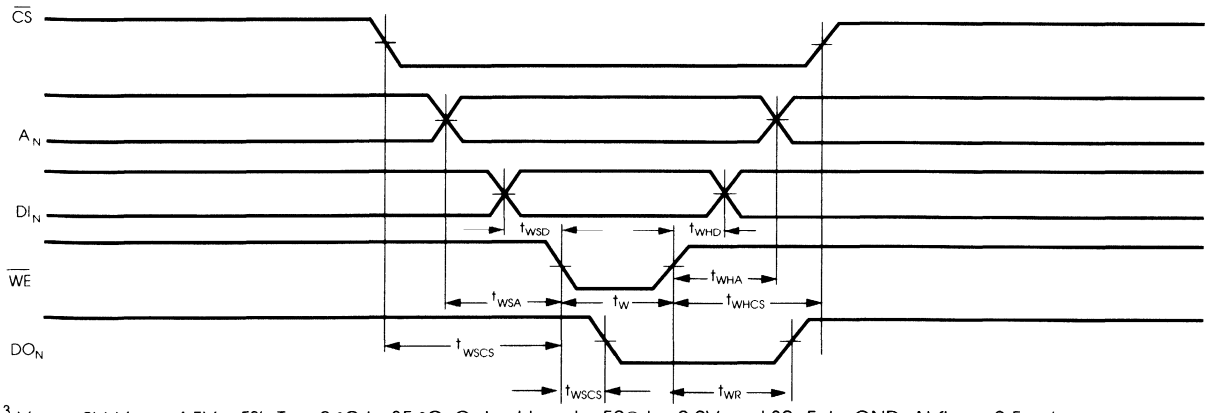




WRITE CYCLE[3]

PARAMETER	SYMBOL	VALUE SSM100484-10 MIN	SSM100484-10 MAX	SSM100484-15 MIN	SSM100484-15 MAX	UNIT
Write Pulse Width	t_W	10		15		ns
Write Disable Time	t_{WS}		5		8	ns
Write Recovery Time	t_{WR}		10		15	ns
Address Set Up Time	t_{WSA}	2		2		ns
Chip Select Set Up Time	t_{WSCS}	2		2		ns
Data Set Up Time	t_{WSD}	2		2		ns
Address Hold Time	t_{WHA}	1		2		ns
Chip Select Hold Time	t_{WHCS}	1		2		ns
Data Hold Time	t_{WHD}	1		2		ns

WRITE CYCLE TIMING DIAGRAM[4]



[3] V_{CC} = 0V, V_{EE} = -4.5V ±5%, T_A = 0 °C to 85 °C, Output Load = 50Ω to -2.0V and 30pF to GND, Airflow ≥2.5 m/s.

[4] All timing measurements referenced to 50% input levels.

OUTPUT RISE AND FALL TIME • CAPACITANCE • AC TEST CONDITIONS

PARAMETER	SYMBOL	VALUE TYP	VALUE MAX	UNIT
Output Rise Time	t_r	2.5		ns
Output Fall Time	t_f	2.5		ns
Input Pin Capacitance	C_{IN}	4		pF
Output Pin Capacitance	C_{OUT}	6		pF

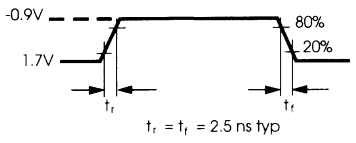


Figure A
Input Pulse Conditions

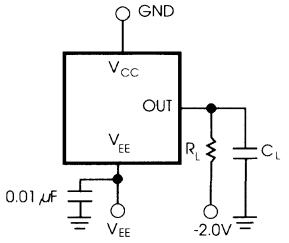
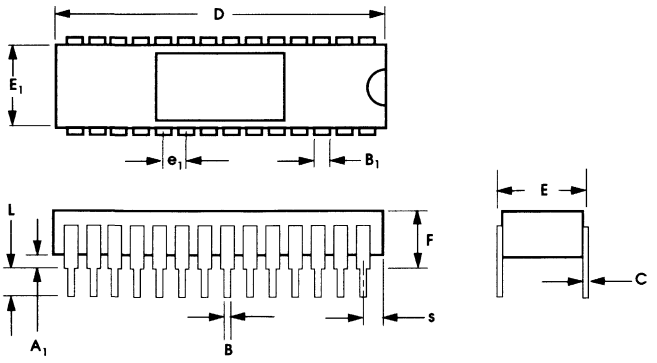


Figure B
Load Circuit

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including probe and stray capacitance)

PACKAGE DIMENSIONS



28 LEAD 400 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.340	1.370
E	.390	.420
E_1	.375	.400
e_1	.090	.110
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	TEMPERATURE RANGE MAX	TEMPERATURE RANGE UNIT
SSM100484-10SC	10ns	28-Pin Sidebraze DIP	0	+85	°C
SSM100484-15SC	15ns	28-Pin Sidebraze DIP	0	+85	°C

NOTE: PLEASE CONTACT FACTORY for information regarding LCC, FLATPACK, and MILITARY TEMPERATURE RANGE devices.

Saratoga Semiconductor

SSM100494

64K 16,384 Words by 4 Bits BiCMOS ECL Static RAM

PRELIMINARY INFORMATION

FEATURES

- **Fast Access Times**
  15/20ns max
- **Fully Compatible with 100K ECL Families**
  Voltage Compensated
  Temperature Compensated
- **Center Power & Ground**
  High Performance
  Improved Noise Margin
- **Industry Standard DIP Package**
- **Low Power Consumption – 200 mA**
- **Pin Compatible with MBM100494**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

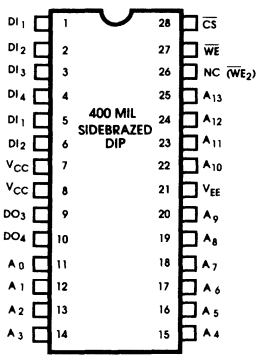
DESCRIPTION

The SSM100494 is a high performance 100K ECL static RAM organized 16,384 words by 4 bits. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

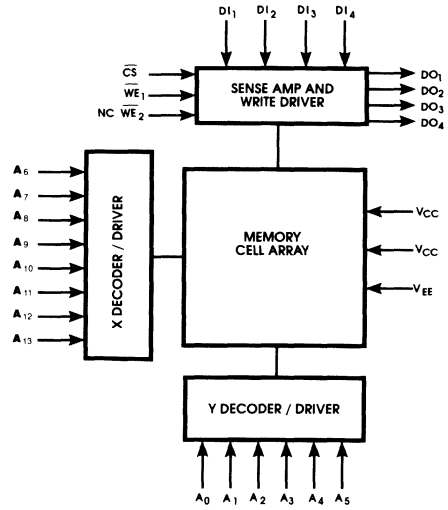
The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input $\overline{CS}$ to its active low condition. When $\overline{CS}$ is low and the two Write Enable inputs ($\overline{WE}_1$ and $\overline{WE}_2$) are also low, information on the Data Inputs (DI_1-DI_4) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0-A_{13}). With $\overline{CS}$ low and $\overline{WE}_1$ or $\overline{WE}_2$ high, the content of the addressed memory cell is transferred to the Data Outputs (DO_1-DO_4). These outputs are in the emitter-follower configuration to permit full wire-ORing capability.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



July 1988

Saratoga Semiconductor

SSM10470

4K 4,096 Words by 1 Bit BiCMOS ECL Static RAM

FEATURES

- **Fast Access Times**
  SSM10470-10: 10ns Address Access
  6ns Chip Select Access
  SSM10470-15: 15ns Address Access
  8ns Chip Select Access
- **Fully Compatible with 10K/10KH Families**
  Voltage Compensated
- **Industry Standard DIP Package**
- **Pin Compatible with Industry Standard**
  MBM10470
  HM10470
  μPB10470
- **Low Power Consumption – 195 mA**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

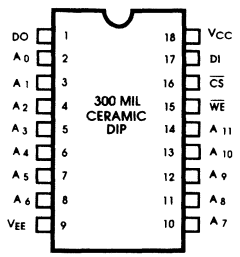
DESCRIPTION

The SSM10470 is a high performance 10K ECL static RAM organized 4,096 words by 1 bit. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input ($\overline{CS}$) to its active low condition. When $\overline{CS}$ is low and the Write Enable input ($\overline{WE}$) is also low, information on the Data Input (DI) is written into the memory cell specified by the 12 bit address placed on the Address Inputs (A_0-A_{11}). With $\overline{CS}$ low and $\overline{WE}$ high, the content of the addressed memory cell is transferred to the Data Output (DO). This output is in the emitter-follower configuration to permit full wire-ORing capability.

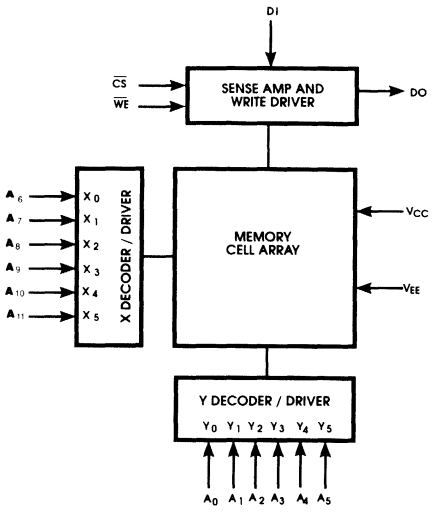
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{11}	Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
DI	Data Input
DO	Data Output
V_{CC}, V_{EE}	Power Supply Pins

FUNCTIONAL BLOCK DIAGRAM



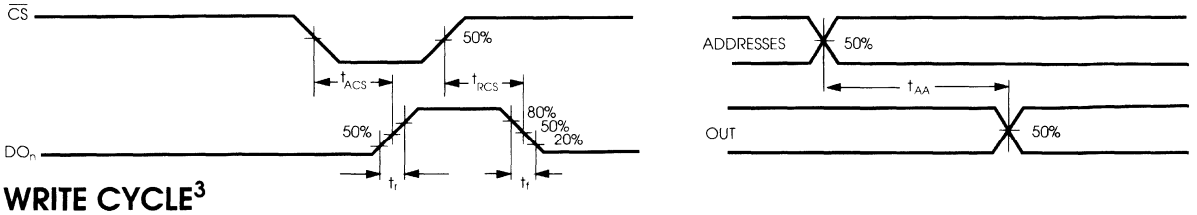
July 1988

AC CHARACTERISTICS

READ CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM10470-10 MIN	SSM10470-10 MAX	SSM10470-15 MIN	SSM10470-15 MAX	UNIT
Address Access Time	t_{AA}		10		15	ns
Chip Select Recovery Time	t_{ACS}		6		8	ns
Chip Select Access Time	t_{RCS}		6		8	ns

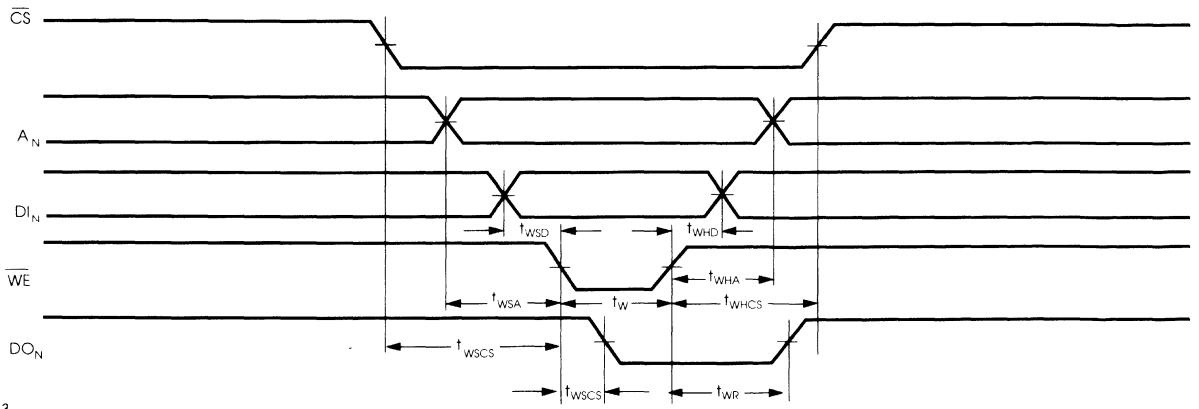
READ CYCLE TIMING DIAGRAMS [4]



WRITE CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM10470-10 MIN	SSM10470-10 MAX	SSM10470-15 MIN	SSM10470-15 MAX	UNIT
Write Pulse Width	t_W	10		15		ns
Write Disable Time	t_{WS}		6		8	ns
Write Recovery Time	t_{WR}		10		15	ns
Address Set Up Time	t_{WSA}	2		2		ns
Chip Select Set Up Time	t_{WSCS}	2		2		ns
Data Set Up Time	t_{WSD}	2		2		ns
Address Hold Time	t_{WHA}	1		2		ns
Chip Select Hold Time	t_{WHCS}	1		2		ns
Data Hold Time	t_{WHD}	1		2		ns

WRITE CYCLE TIMING DIAGRAM [4]



[3] V_{CC} = 0V, V_{EE} = -5.2V ±5%, T_A = 0 °C to 75 °C, Output Load = 50Ω and 30pF to -2V, Airflow ≥ 2.5 m/s.
[4] All timing measurements referenced to 50% input levels.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	DI	DO
Read	L	H	X	DO
Write '0'	L	L	L	L
Write '1'	L	L	H	L
Disabled	H	X	X	L

H = High Voltage Level X = Irrelevant L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Supply Voltage (V_{EE} to GND)	V_{EE}	+0.5	-7.0	V
Input Voltage	V_{IN}	+0.5	V_{EE}	V
Output Current (DC, Output High)	I_{OUT}		-30	mA
Temperature Under Bias	T_A for DIP	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operatior should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Supply Voltage [1]	V_{EE}	-5.46	-5.2	-4.94	V
Ambient Temperature	T_A	0		+75	°C

[1] V_{EE} referenced to V_{CC}.

DC CHARACTERISTICS [2]

SYMBOL	PARAMETER	TEST CONDITIONS	OPERATING TEMPERATURE	VALUE MIN	VALUE MAX	UNIT
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	0°C 25°C 75°C	-1000 -960 -900	-840 -810 -720	mV
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	0°C 25°C 75°C	-1870 -1850 -1830	-1665 -1650 -1625	mV
V_{OHC}	Output High Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	0°C 25°C 75°C	-1020 -980 -920		mV
V_{OLC}	Output Low Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	0°C 25°C 75°C		-1645 -1630 -1605	mV
V_{IH}	Input High Voltage	Guaranteed input voltage high for all inputs	0°C 25°C 75°C	-1145 -1105 -1045	-840 -810 -720	mV
V_{IL}	Input Low Voltage	Guaranteed input voltage low for all inputs	0°C 25°C 75°C	-1870 -1850 -1830	-1490 -1475 -1450	mV
I_{IH}	Input High Current	$V_{IN} = V_{IH}$ max	0°C to 75°C		220	μA
I_{IL}	Input Low Current	$V_{IN} = V_{IL}$ min	0°C to 75°C	-50		μA
I_{IL}	$\overline{CS}$ Input Low Current	$V_{IN} = V_{IL}$ min	0°C to 75°C	0.5	170	μA
I_{EE}	Power Supply Current	All inputs and outputs open	0°C to 75°C	-195		mA

[2] V_{CC} = 0V, V_{EE} = -5.2V, T_A = 0 °C to 75 °C Output Load = 50Ω and 30pF to -2V, Airflow ≥ 2.5 m/s

OUTPUT RISE AND FALL TIME • CAPACITANCE • AC TEST CONDITIONS

PARAMETER	SYMBOL	VALUE TYP	VALUE MAX	UNIT
Output Rise Time	t_r	2.5		ns
Output Fall Time	t_f	2.5		ns
Input Pin Capacitance	C_{IN}	4		pF
Output Pin Capacitance	C_{OUT}	6		pF

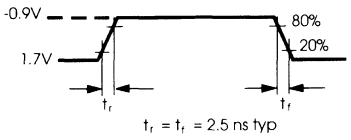


Figure A
Input Pulse Conditions

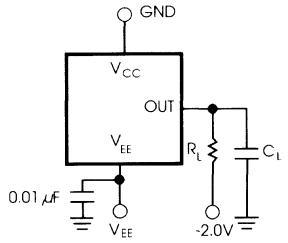
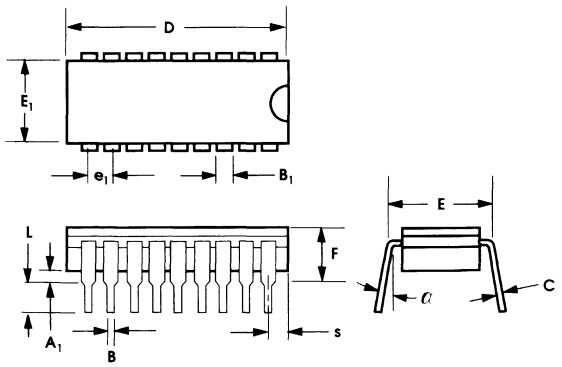


Figure B
Load Circuit

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including probe and stray capacitance)

PACKAGE DIMENSIONS



18 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.045
B	.014	.023
B_1	.050	.065
C	.009	.015
D		.920
E	.300	.320
E_1	.285	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM10470-10CC	10ns	20-Pin CERDIP	0	+75	°C
SSM10470-15CC	15ns	20-Pin CERDIP	0	+75	°C

NOTE: PLEASE CONTACT FACTORY for information regarding LCC, FLATPACK, and MILITARY TEMPERATURE RANGE devices.

Saratoga Semiconductor

SSM10474

4K 1,024 Words by 4 Bits BiCMOS ECL Static RAM

FEATURES

- **Fast Access Times**
  SSM10474-8: 8ns Address Access
  5ns Chip Select Access
  SSM10474-10: 10ns Address Access
  6ns Chip Select Access
  SSM10474-15: 15ns Address Access
  8ns Chip Select Access
- **Fully Compatible with 10K/10KH Families**
  Voltage Compensated
- **Industry Standard DIP Package**
- **Pin Compatible with Industry Standard**
  MBM10474
  HM10474
  μPB10474
- **Low Power Consumption – 240 mA**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

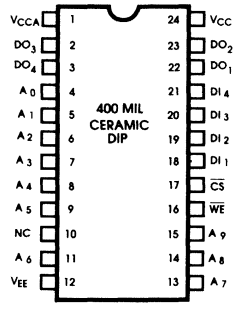
DESCRIPTION

The SSM10474 is a high performance 10K ECL static RAM organized 1,024 words by 4 bits. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input ($\overline{CS}$) to its active low condition. When $\overline{CS}$ is low and the Write Enable input ($\overline{WE}$) is also low, information on the Data Inputs (DI_1 - DI_4) is written into the memory cell specified by the 10 bit address placed on the Address Inputs (A_0-A_9). With $\overline{CS}$ low and $\overline{WE}$ high, the content of the addressed memory cell is transferred to the Data Outputs (DO_1 - DO_4). These output is in the emitter-follower configuration to permit full wire-ORing capability.

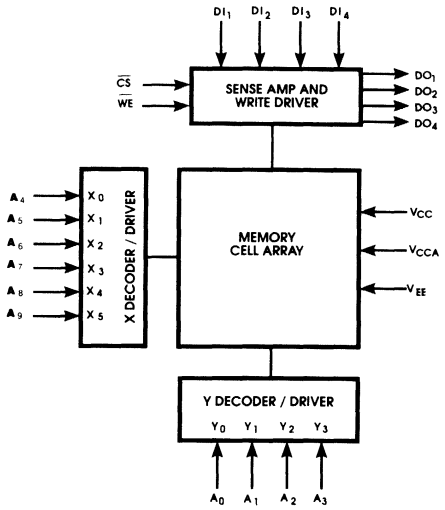
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_9	Address Inputs
DI_1 - DI_4	Data Inputs
DO_1 - DO_4	Data Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Inputs
V_{CC}, V_{CCA}, V_{EE}	Power Supply Pins
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



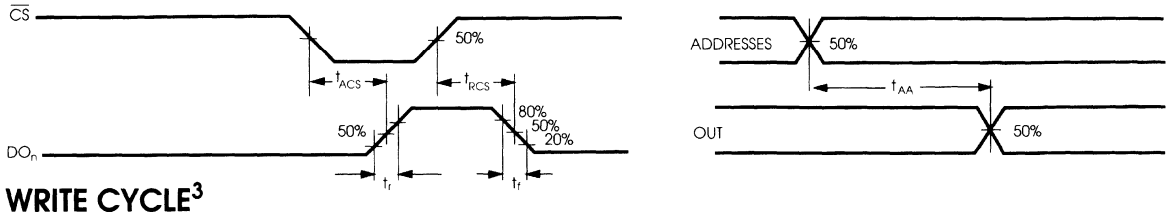
July 1988

AC CHARACTERISTICS

READ CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM10474-8 MIN	SSM10474-8 MAX	SSM10474-10 MIN	SSM10474-10 MAX	SSM10474-15 MIN	SSM10474-15 MAX	UNIT
Address Access Time	t_{AA}		8		10		15	ns
Chip Select Recovery Time	t_{ACS}		5		6		8	ns
Chip Select Access Time	t_{RCS}		5		6		8	ns

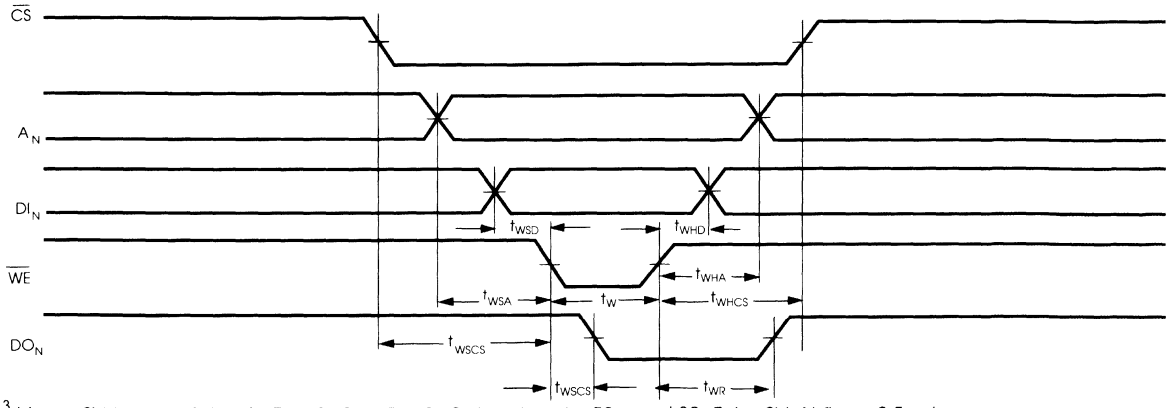
READ CYCLE TIMING DIAGRAMS [4]



WRITE CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM10474-8 MIN	SSM10474-8 MAX	SSM10474-10 MIN	SSM10474-10 MAX	SSM10474-15 MIN	SSM10474-15 MAX	UNIT
Write Pulse Width	t_W	6		8		11		ns
Write Disable Time	t_{WS}		5		6		8	ns
Write Recovery Time	t_{WR}		8		10		15	ns
Address Set Up Time	t_{WSA}	1		1		2		ns
Chip Select Set Up Time	t_{WSCS}	1		1		2		ns
Data Set Up Time	t_{WSD}	1		1		2		ns
Address Hold Time	t_{WHA}	1		1		2		ns
Chip Select Hold Time	t_{WHCS}	1		1		2		ns
Data Hold Time	t_{WHD}	1		1		2		ns

WRITE CYCLE TIMING DIAGRAM [4]



[3] V_{CC} = 0V, V_{EE} = -5.2V ±5%, T_A = 0 °C to 75 °C, Output Load = 50Ω and 30pF to -2V, Airflow ≥2.5 m/s.
[4] All timing measurements referenced to 50% input levels.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	DI_n	DO_n
Read	L	H	X	DO
Write '0'	L	L	L	L
Write '1'	L	L	H	L
Disabled	H	X	X	L

H = High Voltage Level X = Irrelevant L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Supply Voltage (V_{EE} to GND)	V_{EE}	+0.5	-7.0	V
Input Voltage	V_{IN}	+0.5	V_{EE}	V
Output Current (DC, Output High)	I_{OUT}		-30	mA
Temperature Under Bias	T_A for DIP	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Supply Voltage[1]	V_{EE}	-5.46	-5.2	-4.94	V
Ambient Temperature	T_A	0		+75	°C

[1] V_{EE} referenced to V_{CC}.

DC CHARACTERISTICS [2]

SYMBOL	PARAMETER	TEST CONDITIONS	OPERATING TEMPERATURE	VALUE MIN	VALUE MAX	UNIT
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	0°C 25°C 75°C	-1000 -960 -900	-840 -810 -720	mV
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	0°C 25°C 75°C	-1870 -1850 -1830	-1665 -1650 -1625	mV
V_{OHC}	Output High Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	0°C 25°C 75°C	-1020 -980 -920		mV
V_{OLC}	Output Low Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	0°C 25°C 75°C		-1645 -1630 -1605	mV
V_{IH}	Input High Voltage	Guaranteed input voltage high for all inputs	0°C 25°C 75°C	-1145 -1105 -1045	-840 -810 -720	mV
V_{IL}	Input Low Voltage	Guaranteed input voltage low for all inputs	0°C 25°C 75°C	-1870 -1850 -1830	-1490 -1475 -1450	mV
I_{IH}	Input High Current	$V_{IN} = V_{IH}$ max	0°C to 75°C		220	µA
I_{IL}	Input Low Current	$V_{IN} = V_{IL}$ min	0°C to 75°C	-50		µA
I_{IL}	$\overline{CS}$ Input Low Current	$V_{IN} = V_{IL}$ min	0°C to 75°C	0.5	170	µA
I_{EE}	Power Supply Current	All inputs and outputs open	0°C to 75°C	-240		mA

[2] V_{CC} = 0V, V_{EE} = -5.2V, T_A = 0 °C to 75 °C Output Load = 50Ω and 30pF to -2V, Airflow ≥ 2.5 m/s

OUTPUT RISE AND FALL TIME • CAPACITANCE • AC TEST CONDITIONS

PARAMETER	SYMBOL	VALUE TYP	VALUE MAX	UNIT
Output Rise Time	t_r	2.5		ns
Output Fall Time	t_f	2.5		ns
Input Pin Capacitance	C_{IN}	4		pF
Output Pin Capacitance	C_{OUT}	6		pF

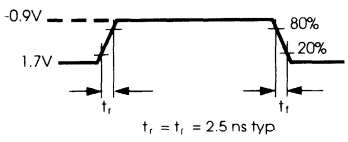


Figure A
Input Pulse Conditions

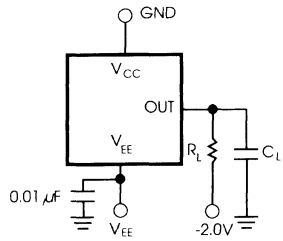
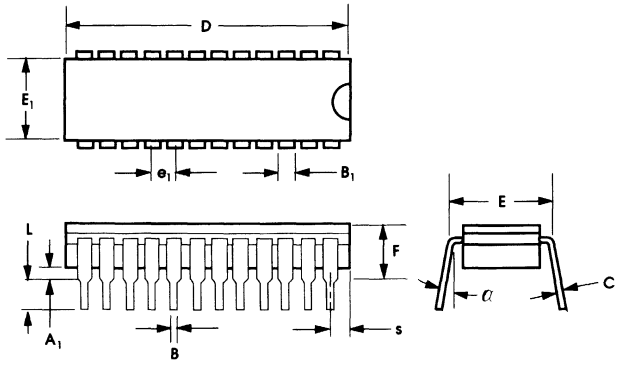


Figure B
Load Circuit

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including probe and stray capacitance)

PACKAGE DIMENSIONS



24 LEAD 400 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.250
E	.380	.420
E_1	.350	.410
e_1	.090	.110
F		.225
L	.125	.200
s		.070
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM10474-10CC	10ns	24-Pin CERDIP	0	+75	°C
SSM10474-15CC	15ns	24-Pin CERDIP	0	+75	°C

NOTE: PLEASE CONTACT FACTORY for information regarding LCC, FLATPACK, and MILITARY TEMPERATURE RANGE devices.

Saratoga Semiconductor

SSM10480

16K 16,384 Words by 1 Bit BiCMOS ECL Static RAM

FEATURES

- **Fast Acess Times**
  SSM10480-10: 10ns Address Access
  5ns Chip Select Access
  SSM10480-15: 15ns Address Access
  8ns Chip Select Access
- **Fully Compatible with 10K/10KH Families**
  Voltage Compensated
- **Industry Standard DIP Package**
- **Pin Compatible with Industry Standard**
  Fujitsu: MBM10480
  Hitachi: HM10480
  NEC: μPB10480
- **Low Power Consumption – 195 mA**
- **SABiC™ BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

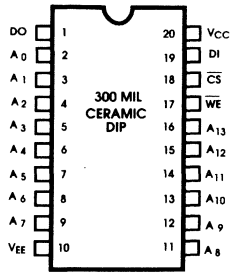
DESCRIPTION

The SSM10480 is a high performance 10K ECL static RAM organized 16,384 words by 1 bit. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC™) wafer fabrication technology. SABiC™ integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input ($\overline{CS}$) to its active low condition. When $\overline{CS}$ is low and the Write Enable input ($\overline{WE}$) is also low, information on the Data Input (DI) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0-A_{13}). With $\overline{CS}$ low and $\overline{WE}$ high, the content of the addressed memory cell is transferred to the Data Output (DO). This output is in the emitter-follower configuration to permit full wire-ORing capability.

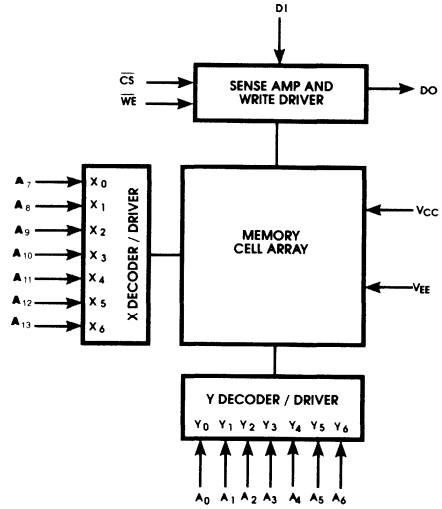
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{13}	Address Inputs
DI	Data Input
DO	Data Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}, V_{EE}	Power Supply Pins

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	DI	DO
Read	L	H	X	DO
Write '0'	L	L	L	L
Write '1'	L	L	H	L
Disabled	H	X	X	L

H = High Voltage Level X = Irrelevant L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Supply Voltage (V_{EE} to GND)	V_{EE}	+0.5	-7.0	V
Input Voltage	V_{IN}	+0.5	V_{EE}	V
Output Current (DC, Output High)	I_{OUT}		-30	mA
Temperature Under Bias	T_A for DIP	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Supply Voltage [1]	V_{EE}	-5.46	-5.2	-4.94	V
Ambient Temperature	T_A	0		+75	°C

[1] V_{EE} referenced to V_{CC}.

DC CHARACTERISTICS [2]

SYMBOL	PARAMETER	TEST CONDITIONS	OPERATING TEMPERATURE	VALUE MIN	VALUE MAX	UNIT
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	0°C 25°C 75°C	-1000 -960 -900	-840 -810 -720	mV
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	0°C 25°C 75°C	-1870 -1850 -1830	-1665 -1650 -1625	mV
V_{OHC}	Output High Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	0°C 25°C 75°C	-1020 -980 -920		mV
V_{OLC}	Output Low Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	0°C 25°C 75°C		-1645 -1630 -1605	mV
V_{IH}	Input High Voltage	Guaranteed input voltage high for all inputs	0°C 25°C 75°C	-1145 -1105 -1045	-840 -810 -720	mV
V_{IL}	Input Low Voltage	Guaranteed input voltage low for all inputs	0°C 25°C 75°C	-1870 -1850 -1830	-1490 -1475 -1450	mV
I_{IH}	Input High Current	$V_{IN} = V_{IH}$ max	0°C to 75°C		220	μA
I_{IL}	Input Low Current	$V_{IN} = V_{IL}$ min	0°C to 75°C	-50		μA
I_{IL}	$\overline{CS}$ Input Low Current	$V_{IN} = V_{IL}$ min	0°C to 75°C	0.5	170	μA
I_{EE}	Power Supply Current	All inputs and outputs open	0°C to 75°C	-195		mA

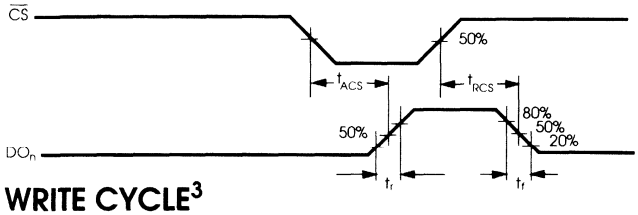
[2] V_{CC} = 0V, V_{EE} = -5.2V, T_A = 0 °C to 75 °C Output Load = 50Ω and 30pF to -2V, Airflow ≥ 2.5 m/s

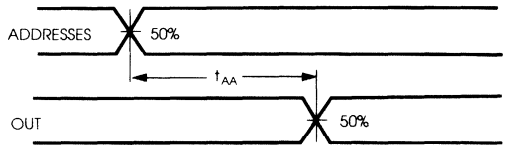
AC CHARACTERISTICS

READ CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM10480-10 MIN	SSM10480-10 MAX	SSM10480-15 MIN	SSM10480-15 MAX	UNIT
Address Access Time	t_{AA}		10		15	ns
Chip Select Recovery Time	t_{ACS}		5		8	ns
Chip Select Access Time	t_{RCS}		5		8	ns

READ CYCLE TIMING DIAGRAMS [4]

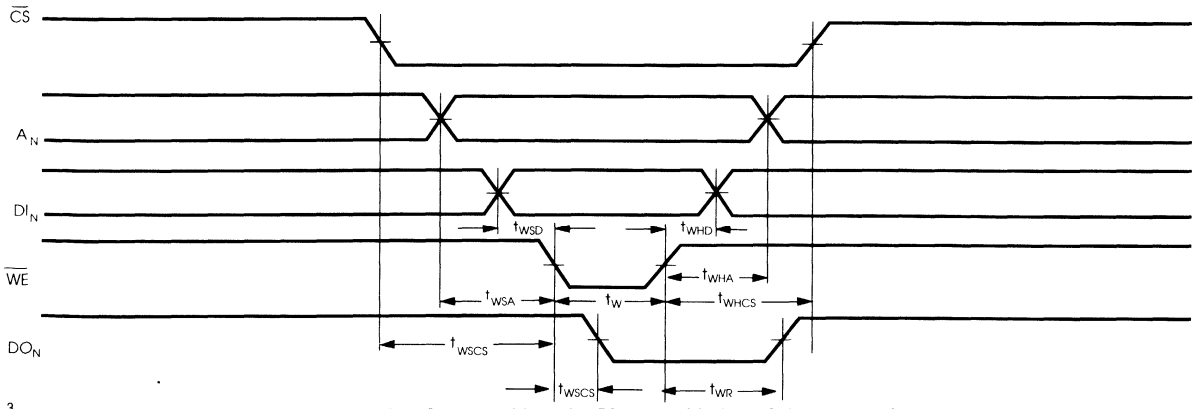




WRITE CYCLE [3]

PARAMETER	SYMBOL	VALUE SSM10480-10 MIN	SSM10480-10 MAX	SSM10480-15 MIN	SSM10480-15 MAX	UNIT
Write Pulse Width	t_W	10		15		ns
Write Disable Time	t_{WS}		5		8	ns
Write Recovery Time	t_{WR}		10		15	ns
Address Set Up Time	t_{WSA}	2		2		ns
Chip Select Set Up Time	t_{WSCS}	2		2		ns
Data Set Up Time	t_{WSD}	2		2		ns
Address Hold Time	t_{WHA}	1		2		ns
Chip Select Hold Time	t_{WHCS}	1		2		ns
Data Hold Time	t_{WHD}	1		2		ns

WRITE CYCLE TIMING DIAGRAM [4]



[3] V_{CC} = 0V, V_{EE} = -5.2V ±5%, T_A = 0 °C to 75 °C, Output Load = 50Ω and 30pF to -2V, Airflow ≥ 2.5 m/s.
[4] All timing measurements referenced to 50% input levels.

OUTPUT RISE AND FALL TIME • CAPACITANCE • AC TEST CONDITIONS

PARAMETER	SYMBOL	VALUE TYP	VALUE MAX	UNIT
Output Rise Time	t_r	2.5		ns
Output Fall Time	t_f	2.5		ns
Input Pin Capacitance	C_{IN}	4		pF
Output Pin Capacitance	C_{OUT}	6		pF

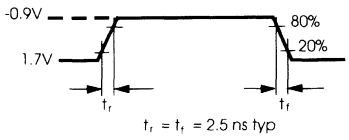


Figure A
Input Pulse Conditions

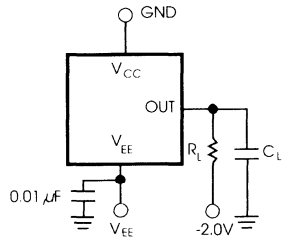
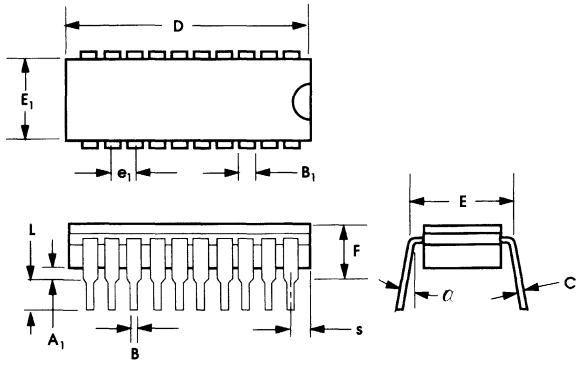


Figure B
Load Circuit

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including probe and stray capacitance)

PACKAGE DIMENSIONS



20 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.060
E	.290	.320
E_1	.220	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM10480-10CC	10ns	20-Pin CERDIP	0	+75	°C
SSM10480-15CC	15ns	20-Pin CERDIP	0	+75	°C

NOTE: PLEASE CONTACT FACTORY for information regarding LCC, FLATPACK, and MILITARY TEMPERATURE RANGE devices.

Saratoga Semiconductor

SSM10484

16K 4,096 Words by 4 Bits BiCMOS ECL Static RAM

FEATURES

- **Fast Access Times**
  SSM10484-10: 10ns Address Access
  5ns Chip Select Access
  SSM10484-15: 5ns Address Access
  8ns Chip Select Access
- **Fully Compatible with 10K/10KH ECL Families**
  Voltage Compensated
- **Industry Standard DIP Package**
- **Pin Compatible with Industry Standard**
  MBM10484
  HM10484
  μPB10484
- **Low Power Consumption – 220 mA**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

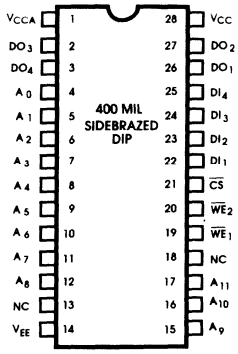
DESCRIPTION

The SSM10484 is a high performance 10K ECL static RAM organized 4,096 words by 4 bits. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input $\overline{CS}$ to its active low condition. When $\overline{CS}$ is low and the two Write Enable inputs ($\overline{WE}_1$ and $\overline{WE}_2$) are also low, information on the Data Inputs (DI_1-DI_4) is written into the memory cell specified by the 12 bit address placed on the Address Inputs (A_0-A_{11}). With $\overline{CS}$ low and $\overline{WE}_1$ or $\overline{WE}_2$ high, the content of the addressed memory cell is transferred to the Data Outputs (DO_1-DO_4). These outputs are in the emitter-follower configuration to permit full wire-ORing capability.

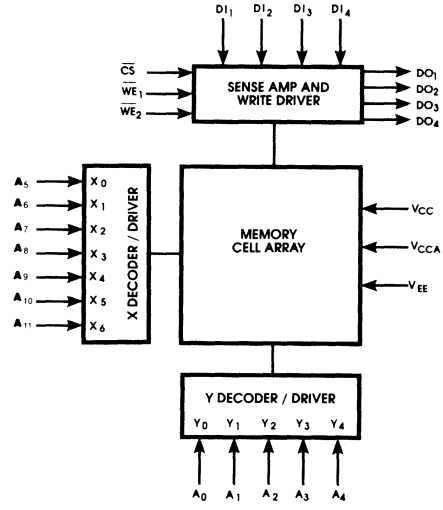
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{11}	Address Inputs
DI_1 - DI_4	Data Inputs
DO_1 - DO_4	Data Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}_1$, $\overline{WE}_2$	Write Enable Inputs
V_{CC}, V_{CCA}, V_{EE}	Power Supply Pins
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



July 1988

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}_1$	$\overline{WE}_2$	DI_n	DO_n
Read	L	H	X	X	DO
Read	L	X	H	X	DO
Write '0'	L	L	L	L	L
Write '1'	L	L	L	H	L
Disabled	H	X	X	X	L

H = High Voltage Level X = Irrelevant L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Supply Voltage (V_{EE} to GND)	V_{EE}	+0.5	-7.0	V
Input Voltage	V_{IN}	+0.5	V_{EE}	V
Output Current (DC, Output High)	I_{OUT}		-30	mA
Temperature Under Bias	T_A for DIP	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Supply Voltage[1]	V_{EE}	-5.46	-5.2	-4.94	V
Ambient Temperature	T_A	0		+75	°C

[1] V_{EE} referenced to V_{CC}.

DC CHARACTERISTICS [2]

SYMBOL	PARAMETER	TEST CONDITIONS	OPERATING TEMPERATURE	VALUE MIN	VALUE MAX	UNIT
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	0°C 25°C 75°C	-1000 -960 -900	-840 -810 -720	mV
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ max or V_{IL} min	0°C 25°C 75°C	-1870 -1850 -1830	-1665 -1650 -1625	mV
V_{OHC}	Output High Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	0°C 25°C 75°C	-1020 -980 -920		mV
V_{OLC}	Output Low Voltage	$V_{IN} = V_{IH}$ min or V_{IL} max	0°C 25°C 75°C		-1645 -1630 -1605	mV
V_{IH}	Input High Voltage	Guaranteed input voltage high for all inputs	0°C 25°C 75°C	-1145 -1105 -1045	-840 -810 -720	mV
V_{IL}	Input Low Voltage	Guaranteed input voltage low for all inputs	0°C 25°C 75°C	-1870 -1850 -1830	-1490 -1475 -1450	mV
I_{IH}	Input High Current	$V_{IN} = V_{IH}$ max	0°C to 75°C		220	µA
I_{IL}	Input Low Current	$V_{IN} = V_{IL}$ min	0°C to 75°C	-50		µA
I_{IL}	$\overline{CS}$ Input Low Current	$V_{IN} = V_{IL}$ min	0°C to 75°C	0.5	170	µA
I_{EE}	Power Supply Current	All inputs and outputs open	0°C to 75°C	-220		mA

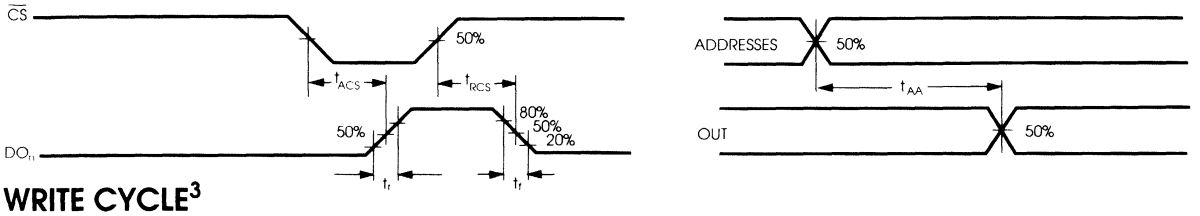
[2] V_{CC} = 0V, V_{EE} = -5.2V, T_A = 0 °C to 75 °C Output Load = 50Ω and 30pF to -2V, Airflow ≥ 2.5 m/s

AC CHARACTERISTICS

READ CYCLE[3]

PARAMETER	SYMBOL	VALUE SSM10484-10 MIN	VALUE SSM10484-10 MAX	VALUE SSM10484-15 MIN	VALUE SSM10484-15 MAX	UNIT
Address Access Time	t_{AA}		10		15	ns
Chip Select Recovery Time	t_{ACS}		5		8	ns
Chip Select Access Time	t_{RCS}		5		8	ns

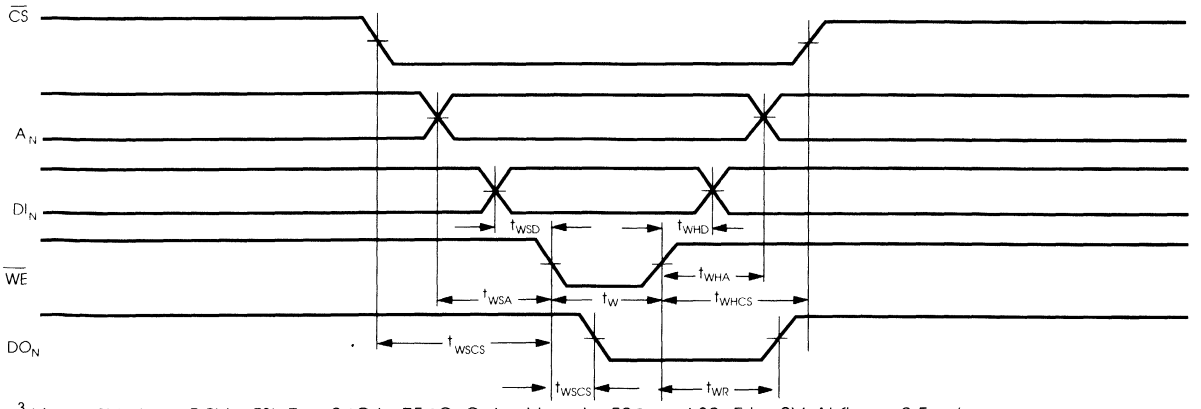
READ CYCLE TIMING DIAGRAMS[4]



WRITE CYCLE[3]

PARAMETER	SYMBOL	VALUE SSM10484-10 MIN	VALUE SSM10484-10 MAX	VALUE SSM10484-15 MIN	VALUE SSM10484-15 MAX	UNIT
Write Pulse Width	t_W	10		15		ns
Write Disable Time	t_{WS}		5		8	ns
Write Recovery Time	t_{WR}		10		15	ns
Address Set Up Time	t_{WSA}	2		2		ns
Chip Select Set Up Time	t_{WSCS}	2		2		ns
Data Set Up Time	t_{WSD}	2		2		ns
Address Hold Time	t_{WHA}	1		2		ns
Chip Select Hold Time	t_{WHCS}	1		2		ns
Data Hold Time	t_{WHD}	1		2		ns

WRITE CYCLE TIMING DIAGRAM[4]



[3] V_{CC} = 0V, V_{EE} = -5.2V ±5%, T_A = 0 °C to 75 °C, Output Load = 50Ω and 30pF to -2V, Airflow ≥ 2.5 m/s.
[4] All timing measurements referenced to 50% input levels.

OUTPUT RISE AND FALL TIME • CAPACITANCE • AC TEST CONDITIONS

PARAMETER	SYMBOL	VALUE TYP	VALUE MAX	UNIT
Output Rise Time	t_r	2.5		ns
Output Fall Time	t_f	2.5		ns
Input Pin Capacitance	C_{IN}	4		pF
Output Pin Capacitance	C_{OUT}	6		pF

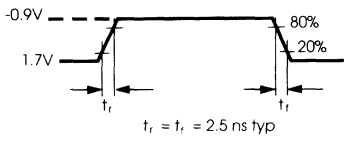


Figure A
Input Pulse Conditions

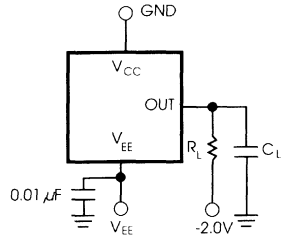
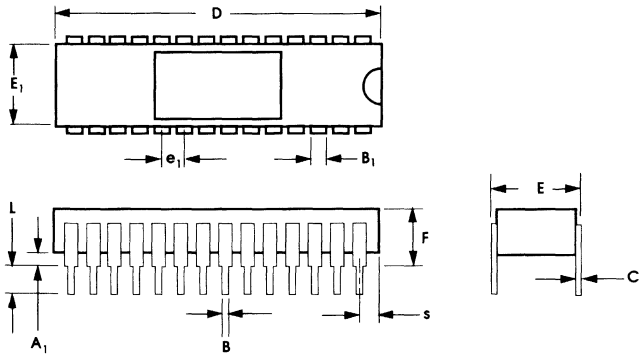


Figure B
Load Circuit

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including probe and stray capacitance)

PACKAGE DIMENSIONS



28 LEAD 400 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

PARAMETER	INCHES MIN	INCHES MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.340	1.370
E	.390	.420
E_1	.375	.400
e_1	.090	.110
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	TEMPERATURE RANGE MAX	TEMPERATURE RANGE UNIT
SSM10484-10SC	10ns	28-Pin Sidebraze DIP	0	+75	°C
SSM10484-15SC	15ns	28-Pin Sidebraze DIP	0	+75	°C

NOTE: PLEASE CONTACT FACTORY for information regarding LCC, FLATPACK, and MILITARY TEMPERATURE RANGE devices.

Saratoga Semiconductor

SSM10494

64K 16,384 Words by 4 Bits BiCMOS ECL Static RAM

PRELIMINARY INFORMATION

FEATURES

- **Fast Access Times**
  15/20ns max
- **Fully Compatible with 10K/10KH ECL Families**
  Voltage Compensated
- **Center Power & Ground**
  High Performance
  Improved Noise Margin
- **Industry Standard DIP Package**
- **Low Power Consumption – 200 mA**
- **Pin Compatible with MBM10494**
- **SABiC BiCMOS Fabrication Technology**
  Low Soft Error Rate
  High Radiation Tolerance
  Military Temperature Range Capability

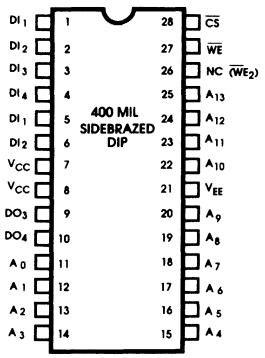
DESCRIPTION

The SSM10494 is a high performance 10K ECL static RAM organized 16,384 words by 4 bits. The device is targeted for use in cache, control store and buffer storage applications in high speed data processing, signal processing and automatic test equipment.

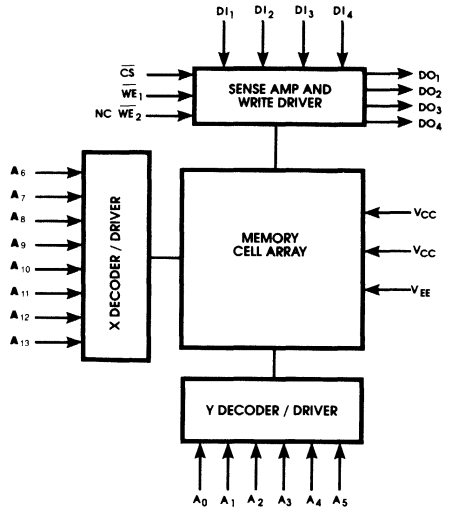
The high speed and low active power consumption of this device, when compared to equivalent bipolar ECL circuits, is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

The device is activated by bringing the Chip Select input $\overline{CS}$ to its active low condition. When $\overline{CS}$ is low and the two Write Enable inputs ($\overline{WE}_1$ and $\overline{WE}_2$) are also low, information on the Data Inputs (DI_1-DI_4) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0-A_{13}). With $\overline{CS}$ low and $\overline{WE}_1$ or $\overline{WE}_2$ high, the content of the addressed memory cell is transferred to the Data Outputs (DO_1-DO_4). These outputs are in the emitter-follower configuration to permit full wire-ORing capability.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM

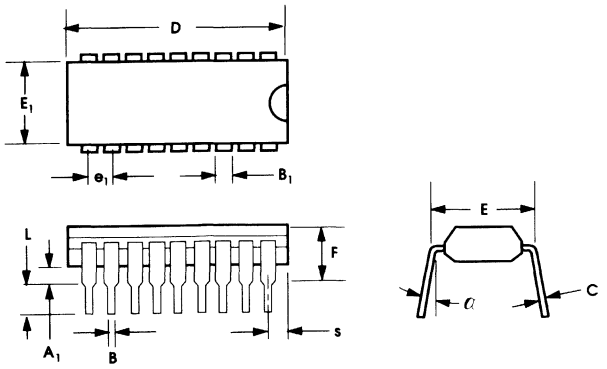


July 1988

PACKAGING

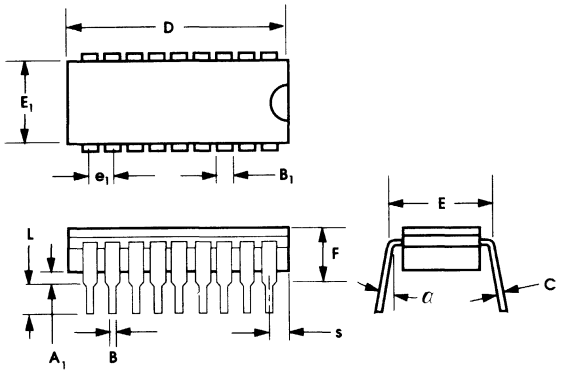
PACKAGING

Package	Products (Section Number)
16-Pin Plastic DIP (300 MIL)	7401 (5), 7403 (5)
18-Pin Plastic DIP (300 MIL)	7402 (5), 7404 (5), 2148 (3), 2149 (3)
20-Pin Plastic DIP (300 MIL)	7413 (5), 6168 (3)
22-Pin Plastic DIP (300 MIL)	4180 (4), 4181 (4), 6170 (3),7188 (3)
24-Pin Plastic DIP (300 MIL)	2150 (3), 6116 (3), 6171 (3), 6172 (3), 7166 (3), 7198 (3)
28-Pin Plastic DIP (300 MIL)	7408 (5), 7409 (5), 7161 (3), 7162(3), 7164 (3),7200(5), 7201 (5), 7202 (5)
28-Pin Plastic DIP (600 MIL)	7200 (5),7201 (5), 7202 (5), 7203 (5), 2152 (4), 2154 (4)
16-Pin CERDIP (300 MIL)	7401 (5), 7403 (5)
18-Pin CERDIP (300 MIL)	2148 (3), 2149 (3), 7402 (5),7404 (5), 10470 (8), 100470 (8)
20-Pin CERDIP (300 MIL)	7413 (5), 6167 (3), 10480 (8), 100480 (8)
24-Pin CERDIP (400 MIL)	10474 (8), 100474 (8)
28-Pin CERDIP (600 MIL)	7200 (5), 7201 (5), 7202 (5), 7203 (5), 2152 (4), 2154 (4)
20-Pin Sidebraze DIP (300 MIL)	6168 (3)
22-Pin Sidebraze DIP (300 MIL)	4180 (4), 4181 (4), 6170 (3), 7188 (3)
24-Pin Sidebraze DIP (300 MIL)	2150 (3), 6116 (3), 6171 (3), 6172 (3), 7166 (3), 7198 (3)
28-Pin Sidebraze DIP (300 MIL)	7408 (5), 7409 (5), 7161 (3), 7162 (3), 7164 (3), 7192 (3), 7193 (3), 7194 (3), 7195 (3)
28-Pin Sidebraze DIP (400 MIL)	10484 (8), 100484 (8), 10494 (8), 100494 (8)
20-Pin Small Outline IC (J-Leadl)	6168 (3)
24-Pin Small Outline IC (J-Lead)	6116 (3), 6170 (3), 6171 (3), 6172 (3)
24-Pin Small Outline IC (Gull Wing)	6116 (3), 6170 (3), 6171 (3), 6172 (3)
28-Pin Plastic DIP Module (600 MIL)	91256 (7)
40-Pin Plastic SIP Module	91257 (7), 91258 (7), 91259 (7), 91260 (7)
40-Pin Plastic ZIP Module	91257 (7), 91258 (7), 91259 (7)
60-Pin Plastic ZIP Module	91512 (7), 91513 (7), 91514 (7)



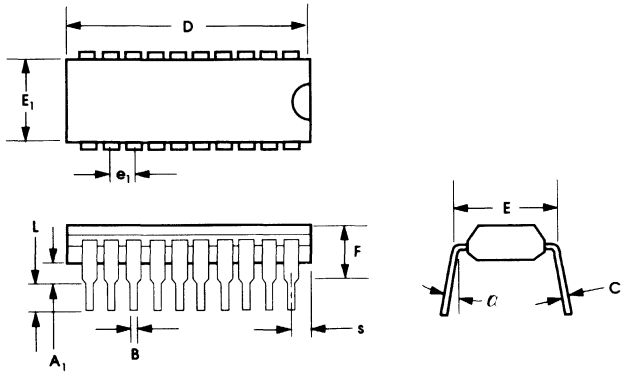
16 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
C	.010	.014
D	.740	.760
E	.280	.300
E_1	.248	.252
e_1	.090	.110
F		.170
L	.125	.145
s	.020	.030
α	0°	15°



18 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

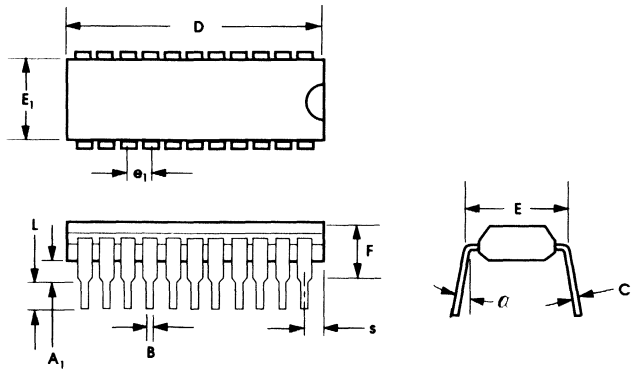
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.045
B	.014	.023
B_1	.050	.065
C	.009	.015
D		.920
E	.300	.320
E_1	.285	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°



20 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

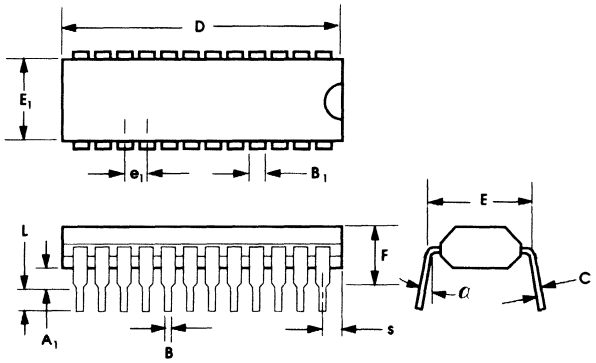
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
C	.008	.012
D	1.023	1.033
E	.280	.300
E_1	.245	.255
e_1	.090	.110
F		.170
L	.125	.135
s	.060	.070
α	0°	15°

PACKAGE DIMENSIONS



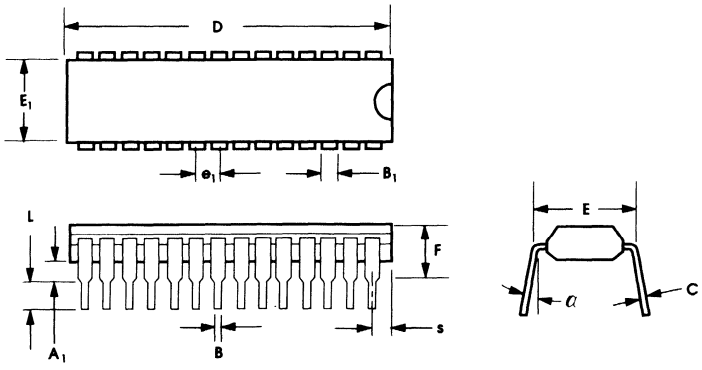
22 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.055
C	.008	.012
D	1.145	1.155
E	.280	.300
E_1	.250	.270
e_1	.090	.110
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



24 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

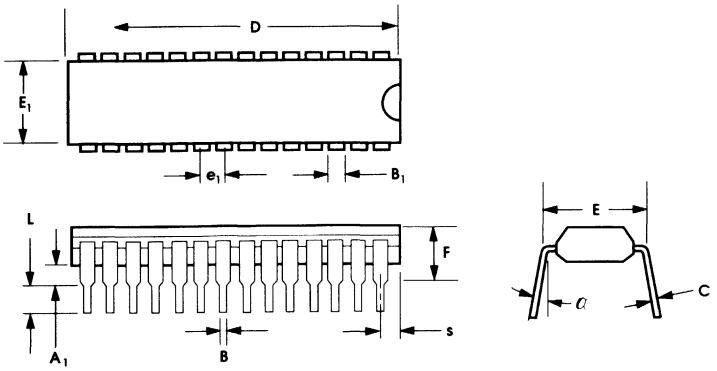
	INCHES	
PARAMETER	MIN	MAX
A_1	.010	
B	.016	.020
B_1	.045	.065
C	.008	.012
D	1.245	1.255
E	.300	.325
E_1	.250	.270
e_1	.095	.105
F		.170
L	.125	.135
s	.070	.080
α	0°	15°



28 LEAD 300 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

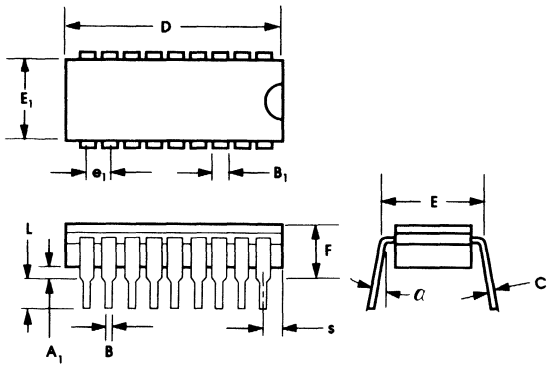
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
C	.008	.012
D	1.345	1.355
E	.300	.325
E_1	.270	.290
e_1	.090	.110
F		.170
L	.125	.135
s	.020	.030
α	0°	15°

PACKAGE DIMENSIONS



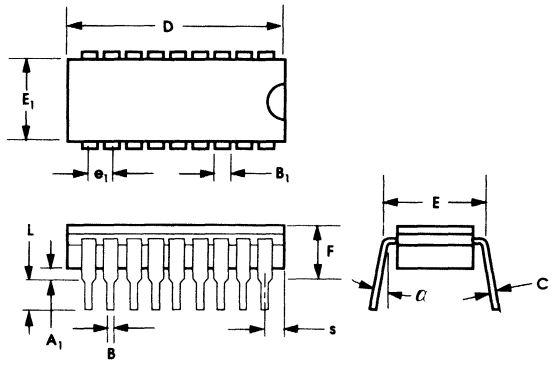
28 LEAD 600 MIL PLASTIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.055	.065
C	.008	.012
D	1.445	1.455
E	.600	.625
E_1	.530	.550
e_1	.090	.110
F		.190
L	.125	.135
s	.070	.080
α	0°	15°



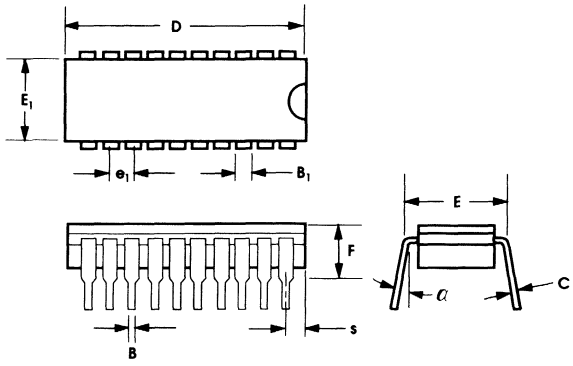
16 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		.840
E	.290	.320
E_1	.220	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°



18 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

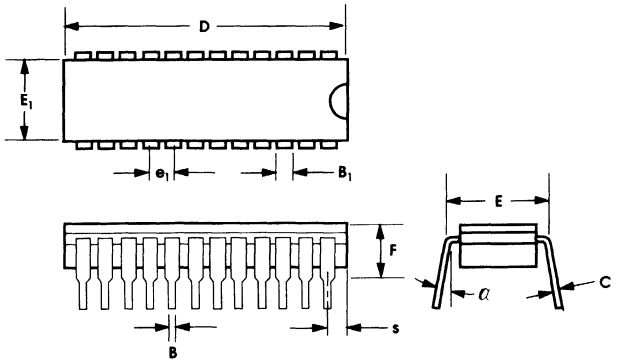
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.045
B	.014	.023
B_1	.050	.065
C	.009	.015
D		.920
E	.300	.320
E_1	.285	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°



20 LEAD 300 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

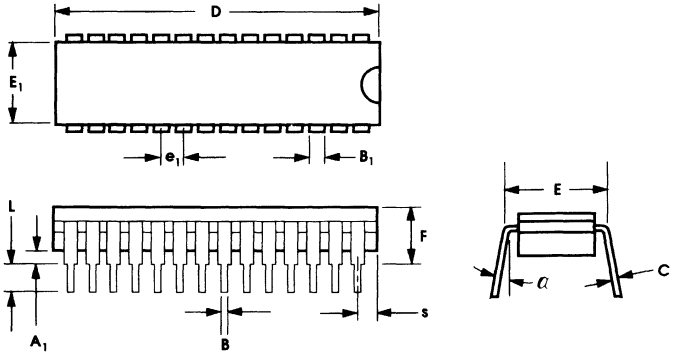
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.060
E	.290	.320
E_1	.220	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080
α	0°	15°

PACKAGE DIMENSIONS



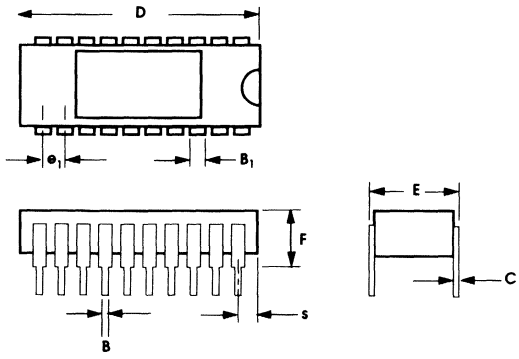
24 LEAD 400 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.250
E	.380	.420
E_1	.350	.410
e_1	.090	.110
F		.225
L	.125	.200
s		.070
α	0°	15°



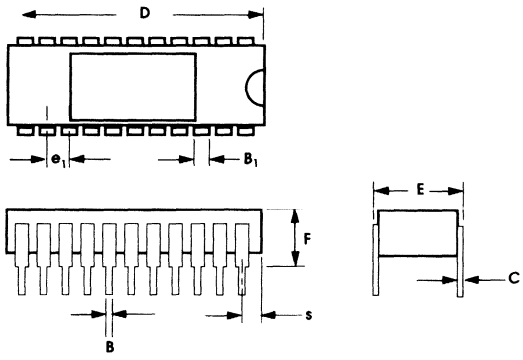
28 LEAD 600 MIL CERAMIC DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.490
E	.590	.620
E_1	.500	.610
e_1	.090	.110
F		.232
L	.125	.200
s		.100
α	0°	15°



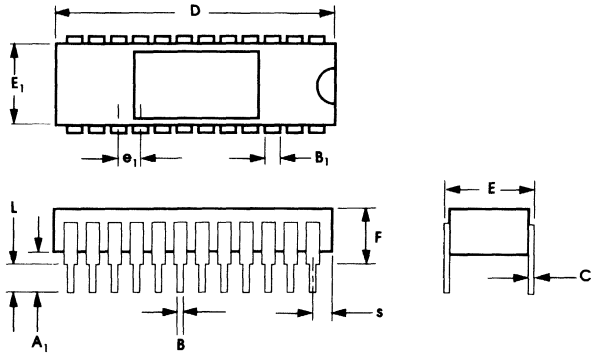
20 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D		1.060
E	.290	.320
E_1	.220	.310
e_1	.090	.110
F		.200
L	.125	.200
s		.080



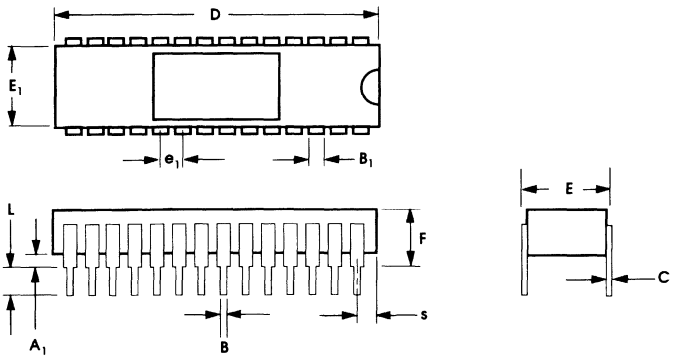
22 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.085	1.115
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100



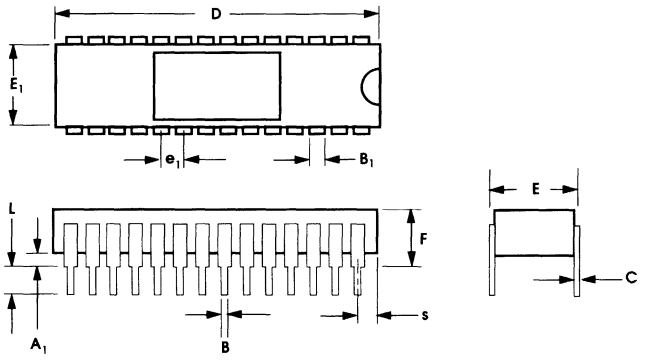
24 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.185	1.215
E	.290	.310
E_1	.285	.305
e_1	.090	.110
F		.232
L	.125	.200
s		.100



28 LEAD 300 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

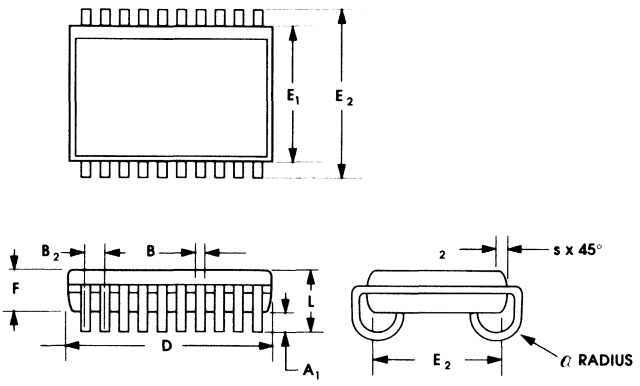
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.385	1.415
E	.285	.305
E_1	.290	.310
e_1	.090	.110
F		.232
L	.125	.200
s		.100



28 LEAD 400 MIL SIDEBRAZE DUAL IN-LINE PACKAGE (DIP)

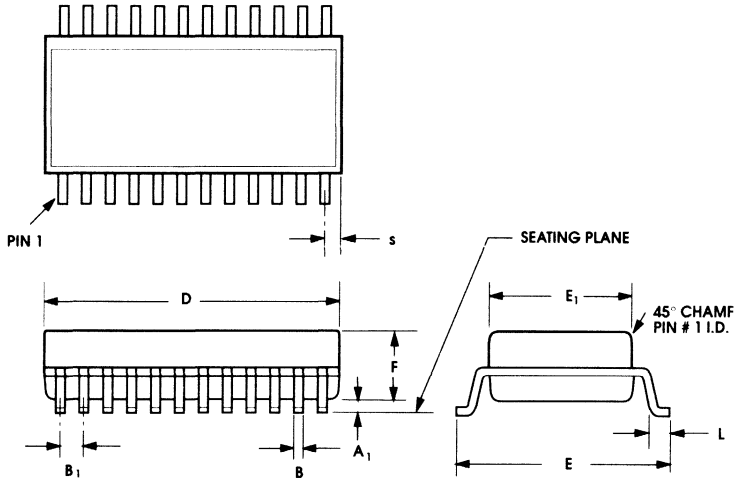
	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.340	1.370
E	.390	.420
E_1	.375	.400
e_1	.090	.110
F		.232
L	.125	.200
s		.100

PACKAGE DIMENSIONS



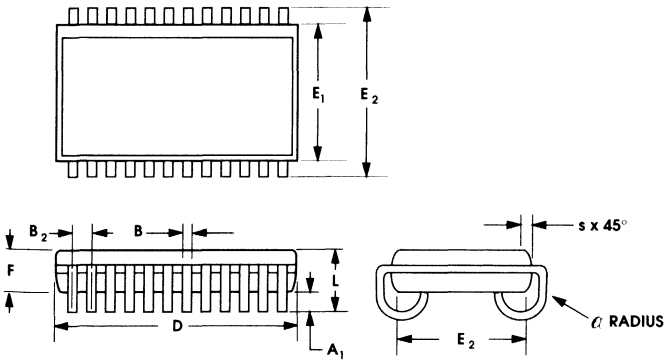
20 LEAD MOLDED SOJ

	INCHES	
PARAMETER	MIN	MAX
A_1	.028	.036
B	.014	.019
B_1	.045	.055
D	.500	.510
E	.335	.347
E_1	.292	.299
E_2	.262	.272
F	.090	.094
L	.120	.140
s	.010	.016
α	.031	.042



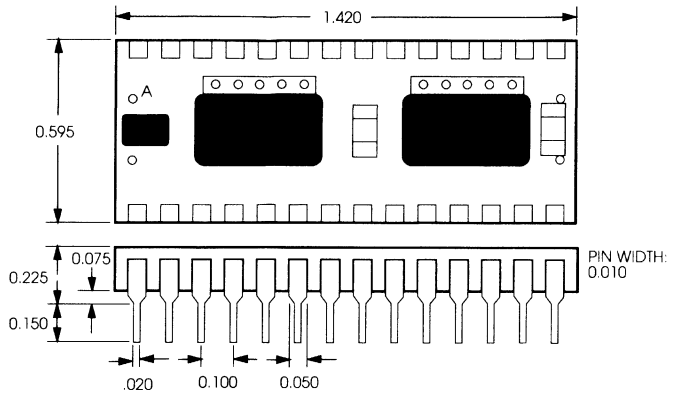
24 LEAD MOLDED SOG

	INCHES	
PARAMETER	MIN	MAX
A_1	.006	.010
B	.014	.019
B_1	.045	.055
D	.602	.612
E	.400	.416
E_1	.292	.299
F	.090	.094
L	.030	.040
s	.026	.032

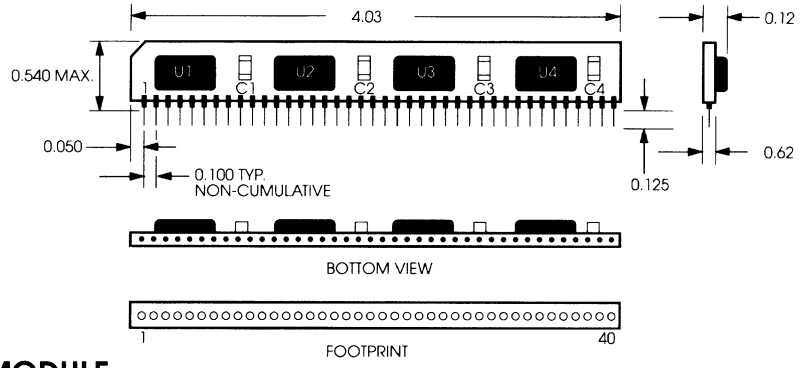


24 LEAD MOLDED SOI

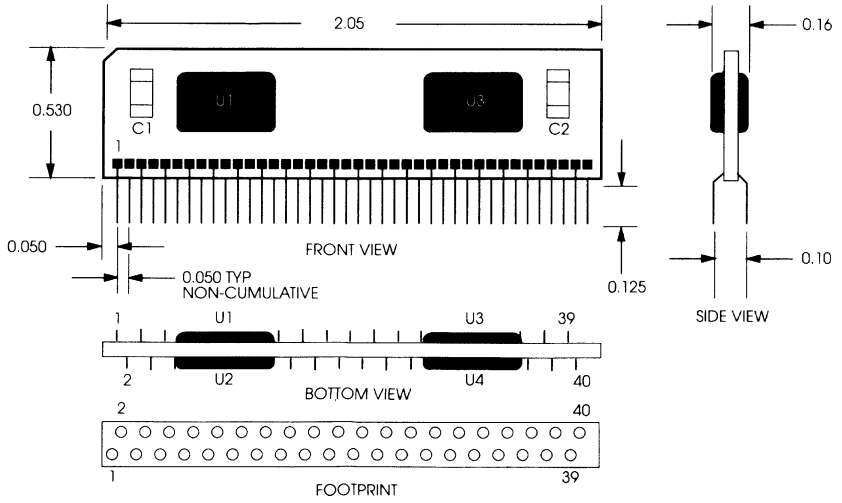
	INCHES	
PARAMETER	MIN	MAX
A_1	.028	.036
B	.014	.019
B_1	.045	.055
D	.602	.612
E	.335	.347
E_1	.292	.299
E_2	.262	.272
F	.090	.094
L	.120	.140
s	.010	.016
α	.031	.042



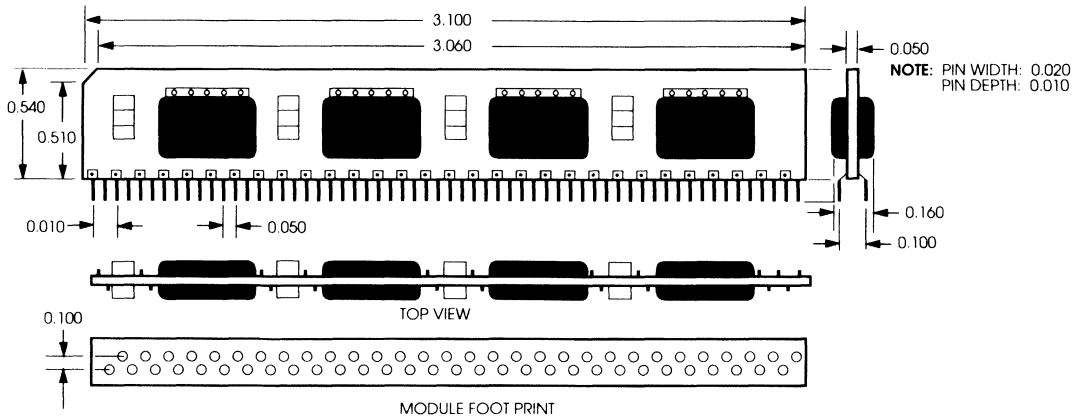
28-LEAD DIP MODULE



40-LEAD SIP MODULE



40-LEAD ZIP MODULE



60-LEAD ZIP MODULE

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